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R&D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS

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FOR

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

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Prepared by
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ABSTRACT

A research and development program was directed toward the development of fabrication technologies for high-speed computer subsystems.

High-yield technologies for fabricating high-speed, high-density microcircuit and two-level microcircuit array structures have been developed and demonstrated. Design requirements for small geometry three-level arrays have also been established.

Multichip high-speed LSI subsystems have been assembled by face-down bonding, and characterized for speed and thermal properties.

Computer aid has been incorporated into a system for designing and generating photomasks for complex high-speed microcircuits. A simple high-speed ECL gate and a complex, high-speed, high-density transistor Read-Only Memory were successfully designed and fabricated to demonstrate the technique.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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I - INTRODUCTION

1.1 PROGRAM OBJECTIVES

The goals of this program were: (1) to establish the technological requirements for achieving very high speed computer systems through fabrication and use of ultrahigh-speed bipolar digital LSI arrays; and (2) to develop methods of subsystem assembly which are compatible with high-speed system performance.

1.2 SCOPE OF REPORT

This report summarizes the work performed from July 1, 1967 to June 30, 1968, on Phase II of the program, "R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The program is an extension of Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF19(628)-5167) which began in July 1964. Previous programs conducted under Subcontract No. 295 were:

- "R&D of a New Class of NPN Silicon Switch Exhibiting UHF Capabilities."
- "R&D Program to Design and Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Times of 1 ns."
- "R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems" - Phase I.

The specific developments of the program are discussed in Sections II through VIII, and the two final sections present conclusions regarding the program and a listing of deliveries made.

1.3 AREAS OF INVESTIGATION

1.3.1 Approach

On this program, the fundamental approach to achieving very high digital subsystem and system operational speeds was to develop compatible LSI techniques around the high-speed microcircuit capability that was developed and demonstrated during a previous program. Digital bipolar microcircuits which operate at 200-400 ps propagation delays (see Eighth Quarterly Summary Report - R&D Program to Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Time of 1 ns.) can be practically made by proper use of small component geometries (2.5 μ) and shallow component diffusions ($\lesssim$ 0.6 μ). However, these short delay times cannot be realized at the systems level when conventional microcircuit packaging and system interconnection techniques are used because of the parasitic loading and signal path delay effects inherent in such an environment. LSI offers the potential of high speeds at the systems level by reducing the number of required packages and the length of system interconnections, thereby providing an

environment for the basic microcircuit gates, flip flops, etc. which has a minimum delaying effect on signal propagation.

The primary program goal was to establish the technological requirements for fabricating, testing and properly implementing ultrahigh-speed LSI microcircuit arrays. Therefore, we concentrated program efforts in a number of related areas, including:

A. Continued development of design principles and fabrication techniques for improving the switching speed-power dissipation properties of the basic microcircuit forms which are used as building blocks in the arrays.

B. Optimizing fabrication yields of these building block microcircuits through improving the yields of the components (especially the high-frequency, small-geometry transistors) which form the microcircuits. As fabrication yields are improved, increasing amounts of high speed logic circuitry can be incorporated in a single monolithic silicon chip, thus allowing a reduction in overall system parasitics, with a consequent improvement in operational speed.

C. Development and optimization of techniques for forming efficient and reliable multilevel interconnection systems for complex microcircuit arrays.

D. Development of techniques for testing complex high-speed arrays to high confidence levels.

E. Development of special packages, in some instances, to accommodate the need for a greater number of leads per package.

F. The development of new techniques for the failure analysis of high-speed arrays. This effort is complicated not only by the small geometries involved but also by the presence of the multilevel metalizations.

A number of vehicles of varying complexities were mutually chosen by Lincoln Laboratory and Philco-Ford and used in the technology development efforts required in the above enumerated areas. These vehicles are described in paragraphs 1.3.2 through 1.3.4.

Large Scale Integration (LSI) can be accomplished by a number of technological approaches. In the pure monolithic approach, a package is required for each chip, and the level of system complexity that is assembled in a given package is determined to a large extent by how complex a chip can be fabricated at practical yields. (This assumes that discretionary wiring is not employed.) A second approach involves the assembly of more than one chip in a package. This multichip subsystem assembly technique, in principle, increases the system

complexity that can be assembled into a single package. Significant program effort has been devoted to the development of a subsystem assembly technique which is compatible with high-speed arrays.

As microcircuit complexities increase and the device manufacturer becomes concerned with larger portions of systems, there arises a greater need for communication and cooperation between the systems people and the device people concerning the design of the subsystem components. This becomes necessary not only from the standpoint of the performance required of the microcircuits or microcircuit arrays, but also from the standpoint of the turn-around time, i.e. the period of time from the microcircuit fabricator's receipt of a subsystem circuit design to his delivery of the equivalent in microcircuit or microcircuit array form. Lincoln Laboratory and Philco-Ford have cooperated throughout the course of this program to promote these ends. Employing design rules and guidance provided by Philco-Ford, Lincoln Laboratory has designed several of the microcircuit and microcircuit array vehicles employed during the program. The two groups have also cooperated in developing computer-aided microcircuit layout design and automatic mask-making techniques.

Increased chip complexity also complicates the testing of arrays to high confidence levels, and the analysis of failures. Lincoln Laboratory personnel have undertaken the development of programs and hardware for computer testing and failure analysis of the various vehicles that have been fabricated on this program.

1.3.2 High-Speed Arrays

Table I lists the high-speed arrays which have been investigated during this program. All are test vehicles intended to present the various challenges of design, fabrication and testing that are characteristic of small-geometry, high-speed LSI arrays.

The Parity Arrays, employing emitter coupled logic, (ECL) were the first vehicles to be investigated. They differ from one another mainly in complexity, as indicated in Table I, and therefore were intended to serve as valuable guides in characterizing process yields and in determining the optimum chip size for small geometry arrays fabricated with our laboratory technologies. The 3-, 9- and 27-Bit Parity Arrays are formed by interconnecting one, four, and 13 parity cells, respectively, through the use of multilevel interconnects. A detailed description of the parity cell was given in the Tenth Interim Report.

TABLE I

HIGH-SPEED ARRAYS USED FOR PROGRAM

Type of Array	Type of Logic	Component Count		Chip Size ($mils^2$)	No. of Pads	Levels of Interconnects
		Transistors	Resistors			
3-Bit Parity	ECL	40	18	30 x 34	12	2
9-Bit Parity	ECL	160	72	45 x 51	23	3
27-Bit Parity	ECL	520	234	90 x 85	59	3
1 x 1 Functional Multiplier	ECL	120	54	60 x 34	15	3
1 x 1 Associative Memory	RTL	21	25	32 x 30		2
4 x 4 Associative Memory	RTL	352	424	96 x 75	26	3
16 x 16 Read Only Memory	E.F. Transistor	256	---	42 x 42	32	2

The 1 x 1 Functional Multiplier Array (FMA) was designed by appropriately interconnecting the components of three parity cells. Basically an exercise in implementing the universal cell approach to LSI, this FMA also served as a vehicle for examining the effect on array yield of what we believed to have been an improved multilevel interconnection design.

The 1 x 1 and 4 x 4 Associative Memory Arrays (AMA) were relatively simple and complex arrays, respectively, employing saturating RTL. Besides representing a microcircuit array design which originated basically with a systems technology group (rather than with device technologists), these arrays were intended to permit investigation of the technology requirements for fabricating high-speed saturated logic arrays.

The Read Only Memory (ROM) is an array which is to be used as a microprogrammer. Designed as a high-speed transistor array (emitter-follower configuration), it was designed to have the flexibility of being programmable at either the wafer level or package level.

1.3.3 Subsystem Assembly Techniques

A second goal of this program was the development of compatible methods of assembly of high-speed digital subsystems.

Conceptually, the method of obtaining the highest speed per circuit stage in a digital system is to maximize the component

density per chip and thereby minimize the number of packages required in the system. Signal delays due to interconnection path lengths and capacitive loading contributed by packages are thereby minimized. Furthermore, because of reduced loading, the consequent reduced requirements for drive circuitry will result in the ability to design more logic onto chips of a given size. Since practical chip size, however, will ultimately be limited by device yields and photomask process limitations, a subsystem assembly technique is required which will make use of the optimized chips (optimized in terms of yield and performance) and yet preserve the high speed inherent to the chips by maintaining minimum signal path lengths and minimum package parasitics. A wafer-chip subassembly approach which employs face-down bonding techniques developed by Philco-Ford* has been investigated.

A face-down bonded version of the 9-Bit Parity Checker employing 3-Bit Parity Arrays as circuit chips, was selected as the vehicle for investigating this technique. The investigation included a characterization of the thermal dissipation and speed properties of the 9-Bit Parity Subsystem Assembly.

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* Kraynak, P. and P. Fletcher, "Wafer-Chip Assembly for LSI," 1967 Internation Electron Devices Meeting, Washington, D.C., October 16-18, 1967.

1.3.4 High-Performance Microcircuits

One of the tasks of the program was to continue developing improved microcircuit design techniques, using relatively simple microcircuit forms as vehicles. Two ECL 3-input gate microcircuit designs were investigated. Both microcircuits are emitter-follower input current switches and have been designed to have a low propagation delay-power dissipation product. One (designated SMX9) emphasizes ultrahigh-speed (<200 ps propagation delay); the other (designated SMX8) emphasizes very low power dissipation (1mW) at moderate speeds (1 to 2 ns propagation delay.)

Special techniques employed to attain the design goals of these microcircuits included the implementation of micron geometries, two-level metalization and tantalum resistors.

A third ECL gate (SMX12) was designed and fabricated to demonstrate the feasibility of a technique for computer-aided microcircuit layout design, which was developed through cooperative efforts between Lincoln Laboratory and Philco-Ford.

II - ARRAY FABRICATION

The implementation of small geometry, high-performance LSI presents many and varied challenges and problems in all phases of array design, fabrication, test and use. With regard to fabrication, high-speed arrays have critical structural requirements and constraints (i.e. small geometries and shallow diffusions) which intensify the normal device yield loss factors. One of the major tasks of this program has been a continuing evaluation of all facets of array design and fabrication (including array photomask fabrication) to minimize the yield loss factors. Yield loss factors can be categorized into two groups:

1. Factors related principally to fabricating array substrates to the microcircuit level or first level of metal.
2. Factors related to fabricating the multilevel interconnection structure.

2.1 ARRAY YIELDS AT THE MICROCIRCUIT LEVEL

Detailed analyses of arrays fabricated throughout this program have led to a number of design and process changes specifically aimed at improving yields at the microcircuit level (especially the transistor yield). It was found during the analyses that yield losses, to varying degrees, were attributable to:

1. Wafer handling
2. Misalignment, misregistration and size variations in photomask patterns
3. Process-induces dislocations in silicon substrates
4. Silicon substrate orientation
5. The metal material employed for microcircuit metalization

2.1.1 Wafer Handling

Special precautionary procedures were instituted to keep wafers completely enclosed except when they are being handled in clean ambients. As a further measure to maintain the ultimate in wafer environment, laminar flow wafer cleaning stations and laminar flow furnace loading ports which are joined by a pass-through have been installed. Figure 1 illustrates the laminar flow enclosures. They not only insure that virtually no room dust can enter and contaminate the diffusion tubes, but also allow wafers to be processed through the critical steps from cleaning through diffusion (or oxidation) under ultraclean environmental conditions.

In addition, the handling of individual wafers was done with special pickup tools wherever possible. These handling aids reduced the defects caused in the photoengraved patterns of wafers

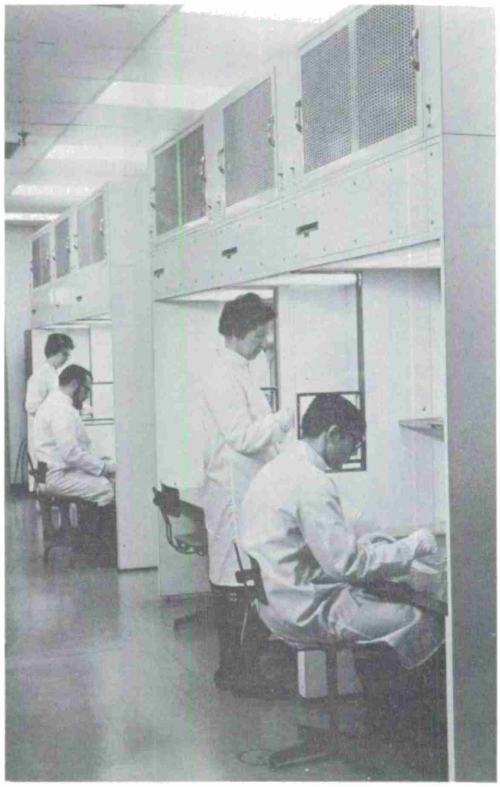


Figure 1. Laminar flow enclosures.

during normal handling in photoresist processing because although the wafers were held by the tools, the wafer surfaces never came in contact with the tools.

2.1.2 Problems Related to Photolithography

Analyses of processed wafers have shown that misregistrations between photomask patterns have also affected yields. Techniques were developed to minimize misregistrations originating during the step-and-repeat operation of mask generation.

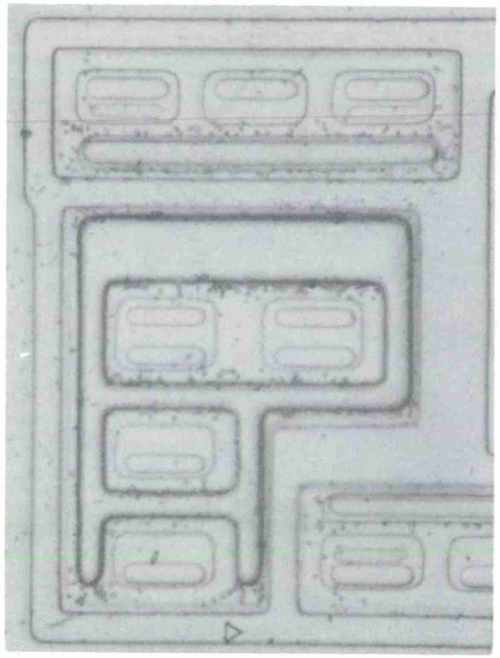
In general, on small geometry microcircuit arrays, the designed patterns and spaces (0.1 mil in many cases) serve as excellent alignment aids in themselves. However it was found that there are cases when auxiliary alignment aids can improve overall alignment accuracies. Appropriate alignment aids were designed, tested, and implemented.

It was found that in certain cases, photomask patterns which are designed to have the same dimensions, do not reproduce identically during photomask fabrication due to pattern-optics interactions. That is, two patterns of identical geometric dimensions can reproduce differently, depending on the pattern environment surrounding the two. The effect has been predominant on metal interconnection masks and has had an adverse effect on microcircuit yields, principally by causing electrical opens. To minimize this effect, certain metalization contact linewidths have been

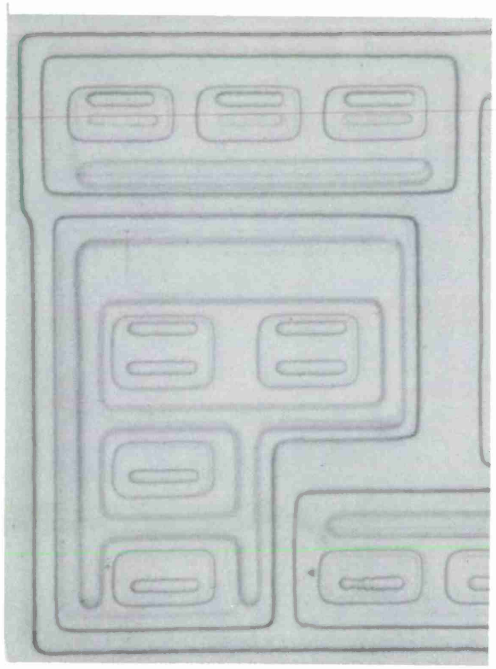
increased to 0.15 and 0.20 mil wherever possible while still maintaining 0.1-mil spacings. This improvement in layout design has reduced the incidence of the described electrical open problem to virtual insignificance.

2.1.3 Process-Induced Dislocations

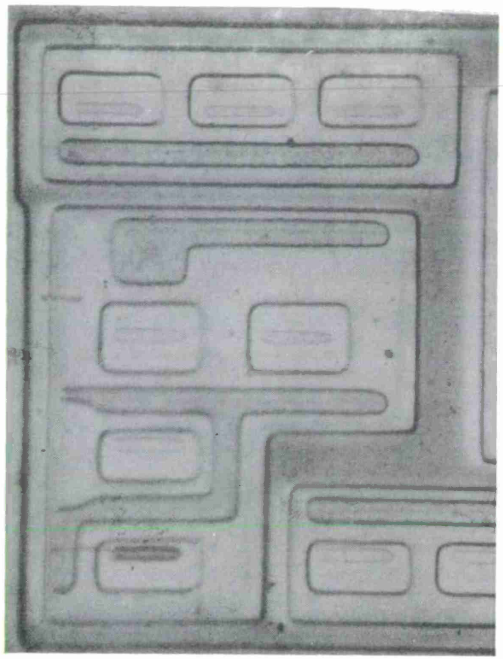
Process-induced dislocations have also been shown to be a major cause of transistor E-C (emitter-to-collector) and E-B (emitter-to-base) shorts and, consequently, a major cause of yield loss in arrays. Excellent correlation was obtained between transistor and array yields and dislocation densities attributable to a high concentration (10^{21} atoms/cc) collector diffusion (feedthrough diffusion) which was performed on early fabricated arrays immediately after oxidation of the epitaxial layer for the purpose of reducing collector resistance in transistors. We found that these dislocations can be avoided either by reducing the doping concentration during this diffusion or by eliminating the diffusion. Figure 2 shows samples of 3-Bit Parity Array wafers representative of the effect of 10^{21} atoms/cc, 10^{20} atoms/cc, and no collector feedthrough diffusion on visibly detectable dislocations, and on measured transistor and array yields. (Dislocations are made visible by subjecting wafers to a Sirtl dislocation etch.)



Wafer No. 12B



Wafer No. 4B



Wafer No. 14B

Wafer No.	Surface Concentration of n+ Collector Feedthrough Diffusion	Transistor Yield
12B	10^{21} atoms/cc	30%
4B	10^{20} atoms/cc	95%
14B	No n+ diffusion	93%

Figure 2. Effect of diffusion-induced dislocations on transistor yield.

All subsequent ECL arrays were processed without the feed-through diffusion.

2.1.4 Silicon Substrate Orientation

A significant yield loss factor which still occasionally affects microcircuit level yields is "buried layer washout and shift." "Buried layer washout" refers to the distortion and, at times, obliteration, of pre-epitaxy diffused patterns which occur during epitaxial layer growth. The "shift" refers to an apparent shift in pre-epitaxial pattern location due to the epitaxial growth process. This phenomenon makes difficult the proper location of post-epitaxy device and isolation regions and, in the worst cases, has resulted in device-to-isolation shorts and poor isolation. This is a particularly harmful yield loss factor in that it can cause a 100% loss on the wafers that are affected. Techniques for minimizing buried layer washout and distortion have been and continue to be investigated. One technique which has resulted in minimized washout involves increasing the off-orientation angle on ⟨111⟩ substrate wafers being used from the conventionally used 1° - 2°, to 3° - 5°, with the surface normal directed toward the ⟨110⟩ direction. We found, however, that pattern shift is not eliminated by this technique; therefore, to obtain the precise alignment of post-epitaxy pattern

to buried layer patterns that is made necessary by our high component density design rules, each wafer ingot must be characterized in terms of pattern shift.

2.1.5 Microcircuit Metalization

During the first half of the program, we found it necessary to use a bimetal film for the first level of metalization in multilevel arrays to minimize interlevel contact resistance. Analyses of array properties have suggested, however, that the bimetal film, consisting of aluminum and an interface metal, was affecting emitter-base diode quality. This was verified when wafers from the same lot were metalized using an all-aluminum film. Inasmuch as our multilevel process has since been developed to allow aluminum alone to be employed as the first-level metal, the use of the bimetal film has been discontinued.

Implementation of the appropriate technology improvements discussed in this subsection resulted in such an improvement in transistor yields that yields greater than 90% were consistently obtained thereafter. Transistor yield was sampled by measuring 100 randomly selected transistors on each wafer at the microcircuit level, using a special test metalization pattern which is replaced by the array cell metal pattern after the testing. Table II shows the improved transistor yields measured in this manner on four of the first 3-Bit Parity Array wafers to be

fabricated using the improvements cited above. Transistor yields continued at these levels throughout the remainder of the program.

TABLE II

TRANSISTOR YIELDS MEASURED ON ARRAY WAFERS MADE WITH IMPROVED TECHNOLOGY

Wafer No.	Transistor Yield	Failure Causes		
		E-B Leakage	E-C Leakage	C-B Leakage
14D	92%	6%	1%	1%
17A	97%	2%	1%	0%
17B	96%	0%	4%	0%
17C	97%	1%	2%	0%

2.2 MULTILEVEL INTERCONNECTION PROCESSING YIELDS

In general, the two major yield limiting factors in the processing of multilevel metalization structures are: (1) Insulator defects, which lead to interlevel metal shorts, and (2) high resistance or electrically open vias, which in the extreme cases result in some portions of the arrays not being interconnected. The net effect of the smaller size of small-geometry arrays on these yield factors is to minimize the insu-

lator defect problem due to reduced conductor crossover areas. This stems from the narrower metal linewidths and shorter metal runs. However, due to topographical features unique to small geometry arrays, there can be a counteracting detrimental effect on the inherent quality of deposited insulators employed in multilevel structures.

In small-geometry arrays, the problem of via resistance is aggravated because the via crossectional areas are typically 1/3 to 1/10 the area of vias in larger geometry arrays. Whereas larger geometry LSI arrays employ vias with a minimum area of 0.25 mil^2 to 0.375 mil^2, the small-geometry arrays we have designed employ vias with minimum areas of 0.03 mil^2 to 0.09 mil^2.

2.2.1 Insulator Processing - Defect Density Control

There are two categories of defects experienced in insulating films employed in multilevel structures:

1. Defects which are generated during film formation (intrinsic defects);
2. Defects which are generated during via photoengraving.

2.2.1.1 Intrinsic Defects

There are four major determinants of the intrinsic quality of deposited insulators:

1. The insulator material itself.

2. The method employed to deposit the insulator film.
3. The method employed to clean the substrates prior to deposition.
4. Topography of the substrates.

SiO_2 was chosen as the insulator material because of its compatibility with the remainder of the microcircuit system, and because of its inherently fine insulator qualities. A review of possible methods for depositing SiO_2 led to the selection of r-f sputtering and vapor deposition (oxidation of silane), both of which are low temperature ($\leq 400^\circ$ C) processes, as the most promising methods. Experiments with films deposited by both methods revealed that vapor deposited films consistently had superior intrinsic insulator qualities (lower pinhole densities.) As an example, when comparing 7000 Å SiO_2 layers deposited on bare silicon substrates, area per defect quantities (inverse pinhole density) ran as high as 150,000 $mils^2$/defect for vapor deposited SiO_2, but only 6000 $mils^2$/defect for r-f sputtered SiO_2. Consequently, vapor deposited SiO_2 was employed on all multilevel arrays fabricated on this program. Experiments with vapor deposited films further indicated that the lower the stress in the deposited films, the lower were pinhole densities. As an example, reducing film stress from levels of 3-4 x 10^9 dyne/cm^2 to

the 1.5 x 10^9 dyne/cm^2 level resulted in an increase in area/defect value from the 10,000 - 20,000 $mils^2$/defect range to the 20,000 - 25,000 $mils^2$/defect range. A further reduction of stress to the level of 1 x 10^9 dynes/cm^2 increased area/defect values to greater than 40,000 $mils^2$/defect. (These film defect properties were recorded on test structures simulating array substrate topographies.) Film growth techniques which yielded the lowest stresses indicated above were developed during the third quarterly period, and were employed on all arrays fabricated during remainder of the program.

The defect properties of silane deposited films were found to be strongly dependent upon substrate topography. Oxide defects occur more frequently on an aluminized silicon substrate than on a bare silicon substrate. In large-geometry arrays, defects occur more frequently along aluminum pattern peripheries than over flat portions of aluminum. As an example, on capacitor test structures employing a first-level microcircuit metal 5000 Å thick and a 7000 Å insulator film, we found that there existed 1.5 times as many defects per mil of aluminum conductor periphery as there were defects per $mils^2$ of aluminum area. We found that insulators employed in 2-level small-geometry arrays are more susceptible to periphery defects than are those used in large-geometry arrays due to the unique topographies of small-geometry microcircuit structures. Since the oxide cuts and contacting

metalization are, in many cases, the same width on the microcircuit level of small-geometry arrays, topographical voids or crevices can be created due to small variations in pattern sizes and registrations. This is illustrated in Figure 3. Impurities and/or volatiles can be trapped in these voids prior to insulator deposition, to cause defects in the insulator deposited on them.

The method of cleaning substrates prior to vapor deposition of SiO_2 also strongly affects the integrity of the films. As might be expected, insulator films on substrates with topographies are more sensitive to cleaning procedures from the standpoint of pinholes than films on substrates without topographies. Again, because of their unique topographies, small-geometry array substrates require most thorough cleaning prior to insulator deposition.

Figures 4 and 5 illustrate test capacitor structures employed to study the defect properties of deposited insulators. The structure of Figure 4 simulates the substrate topography existent beneath the first-level insulator of small-geometry arrays. The structure of Figure 5 simulates the substrate topography existent beneath the second-level insulator of small-geometry arrays, as well as the substrate topography beneath all levels of more conventional arrays.

Details of the method in which these capacitor test structure

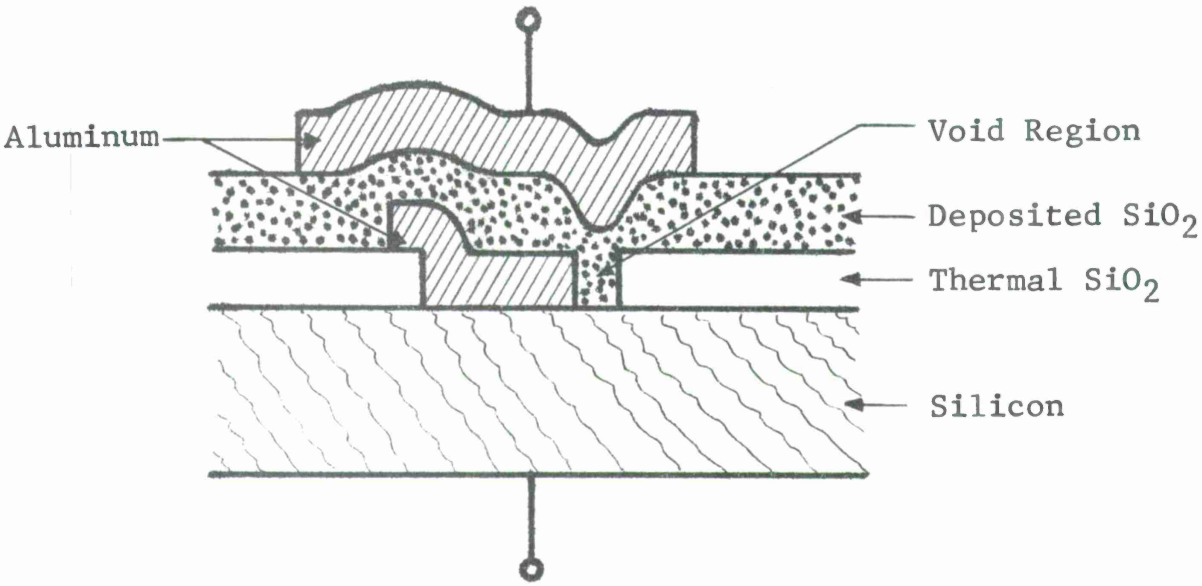


Figure 3. Sketch of cross section of a small geometry array structure in the vicinity of contact cut.

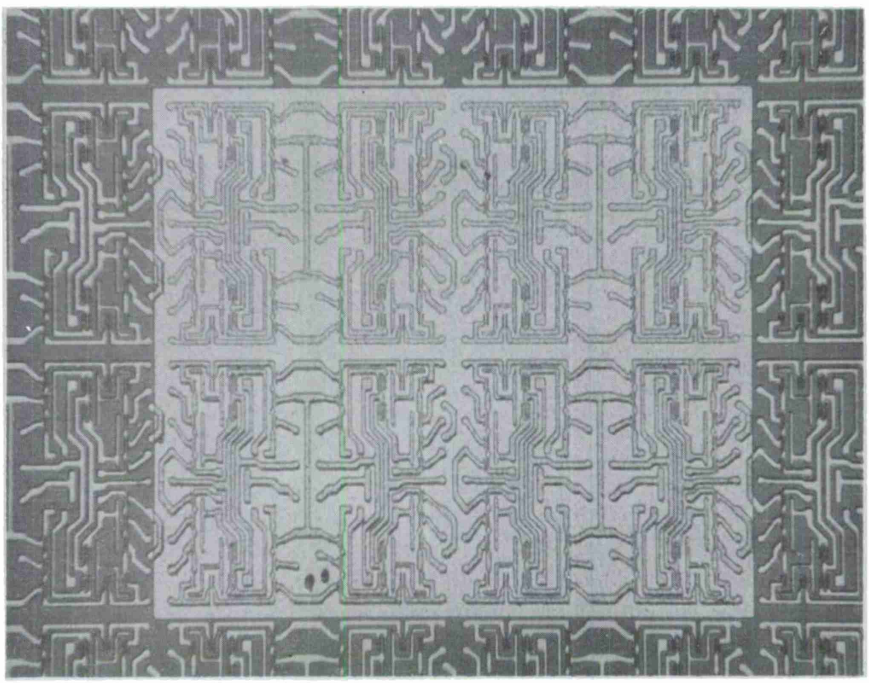


Figure 4. Top view of small geometry array insulator test structure.

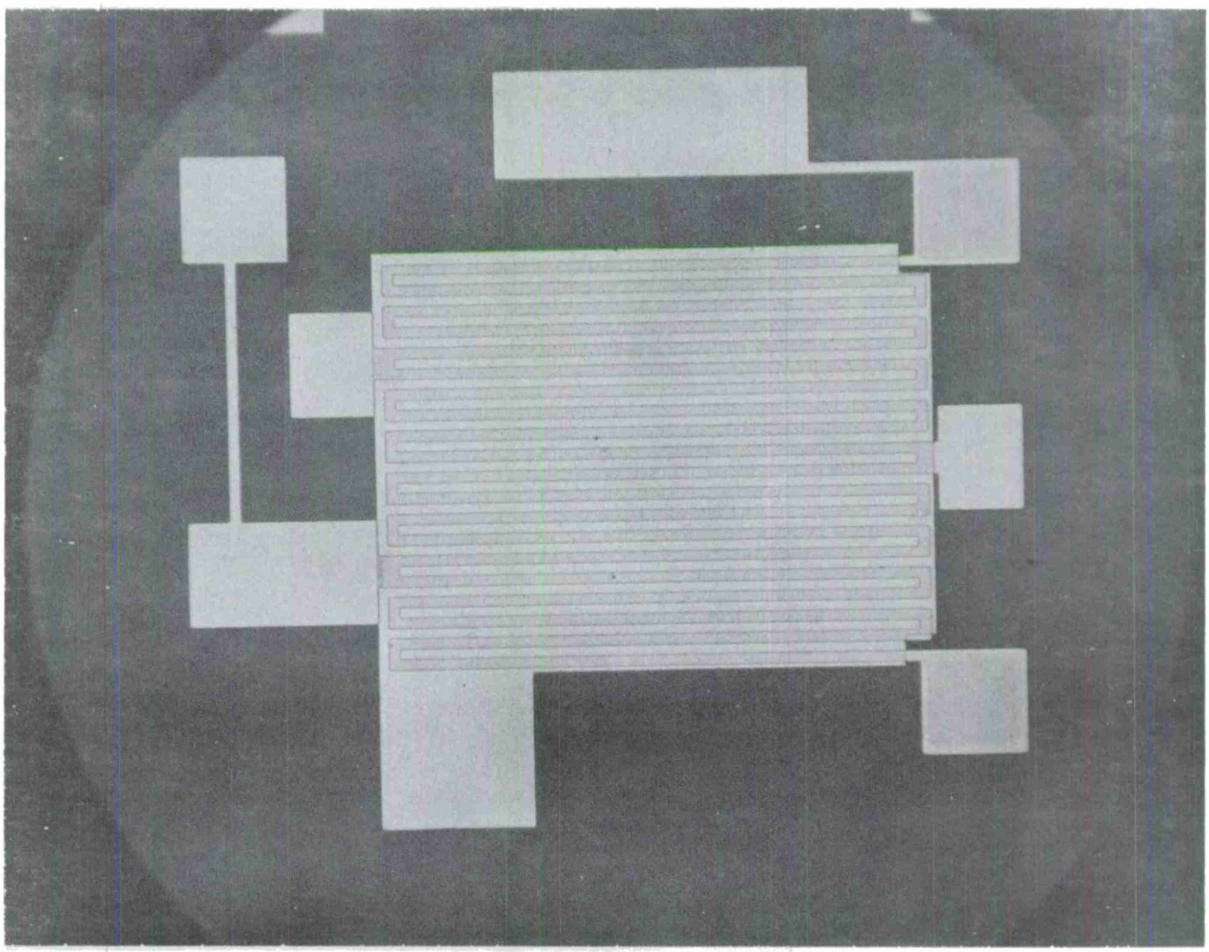


Figure 5. Test capacitor structure.

yields are employed to quantitatively evaluate the quality of insulator films are presented in subparagraph 2.2.2.1 of the Twelfth Interim Report.

2.2.1.2 Defects Generated by Photoengraving

Defects can be generated in insulator layers during photoengraving because of a number of factors, i.e., inherent pinholes in the photoresist, opaque defects on the photomasks, and photoresist defects created by the contact exposure operation. Defects from all these sources have been minimized by a redundant photoengraving process which was developed during this program. This process employes two separate photoresist layers, two separate via masks and two separate etching operations, each etching timed to remove slightly more than half of the insulator thickness in via regions. The success of this method stems from the very low probability that the defects peculiar to the separate photomasks, resist layers, and contact exposure operations will occur at the same location.

2.2.2 Via Photoengraving and Via Resistance Control

Circuit interconnections between the various levels of metalization in arrays are made through holes, commonly called "vias," photoengraved in the insulating layers which insulate consecutive metal layers. Since aluminum is the most widely used

metalization in microcircuits, and the favorable reliability properties of aluminized microcircuits are documented, it is desirable to employ aluminum for all levels of metalization in arrays. However, aluminum is a metal that easily oxidizes and therefore high resistance and open via paths can occur if the aluminum metalization layers are not properly processed. Furthermore, via problems also result if the insulating layers and vias are not properly processed.

Early in this program, yields of all small-geometry arrays being fabricated (two-level and three-level arrays) were seriously affected by high resistance and open vias. The problem was attributed to oxidation of the first-level aluminum during processing subsequent to first-level metal evaporation, and to the presence of residual insulator material in some vias brought about by uneven etching of the insulator material. The effects of both of these factors were exaggerated by the small size of the vias; this fact became evident when processing sequences which were effective in producing low-resistance large-area vias (0.5 mil diameter) were insufficient to do the same with the 0.20- and 0.25-mil diameter vias employed in the small-geometry arrays. A number of different techniques for eliminating the proposed thin aluminum oxide film were investigated. (Details are given in the subparagraph 2.2.2.2 of the Twelfth Interim Report.)

None of the methods were successful. As a result, it became necessary to employ a two-layer metal film for first-level metal, in which aluminum was coated over with a barrier metal which would prevent the aluminum from oxidizing and still either not form an insulating oxide of itself or form an oxide which is easily reduced by aluminum. An aluminum-nickel bimetal film was found to be effective in yielding relatively low-resistance small-area vias. Structures were made in which via resistance was only 0.32- to 0.35-Ω for via sizes on the order of 0.023 mil^2.

Use of the bimetal film was instrumental in the fabrication of the first wafer of two-level small-geometry arrays with trouble-free vias. Array yield on that wafer of 3-Bit Parity Arrays was 5.3%. The bimetal film, however, was treated as only an interim solution to the via problem, because we believed that the simpler all-aluminum metal system was more ideal from the standpoint of reliability. Furthermore, evidence was gathered which indicated that the bimetal film was affecting emitter-base diode quality in arrays. During the third quarter of the program, continued efforts at implementing an all-aluminum system were successful. By optimizing the redundant via etching process and aluminum evaporation techniques, it became possible to return to an all-aluminum two-level metal interconnection system (containing the same size vias), with no apparent increase in via resistance.

Not only did the new process reduce the effect of any oxide which might form on the first-level aluminum, but it also overcame the tendency of vias to etch nonuniformly. The improved all-aluminum two-level interconnection process led to as much as a five times increase in yields of 3-Bit Parity Arrays. It also permitted the successful fabrication of other 2-level arrays, containing as many as 256 small-area vias.

III - HIGH-SPEED ARRAYS

A number of two-level and three-level arrays were employed as study vehicles on this program. This section discusses each of these arrays in light of the technology developments pertinent to each.

3.1 TWO-LEVEL ARRAYS

3.1.1 3-Bit Parity Array

The 3-Bit Parity Array has 58 components and two levels of metalization, and employs Emitter Coupled Logic. A photomicrograph of this array is shown in Figure 6. Figure 7 shows the schematic diagram of the array. Realization of 3-Bit Parity Arrays required a capability to fabricate transistors at yields greater than 85% and a capability to fabricate a two-level interconnection structure which employs vias possessing a cross-sectional area of 0.03 to 0.05 mil^2 (31 vias per array).

Early attempts at fabricating the 3-Bit Parity Array were unsuccessful due to the microcircuit level yield problems, and the via resistance problems described in paragraphs 2.1.1 and 2.2.2. However, after the improvements in processing technology described in those paragraphs raised transistor yields to levels in excess of 90% and provided the ability to fabricate small-area vias at high yield, 3-Bit Parity Arrays were fabricated at high

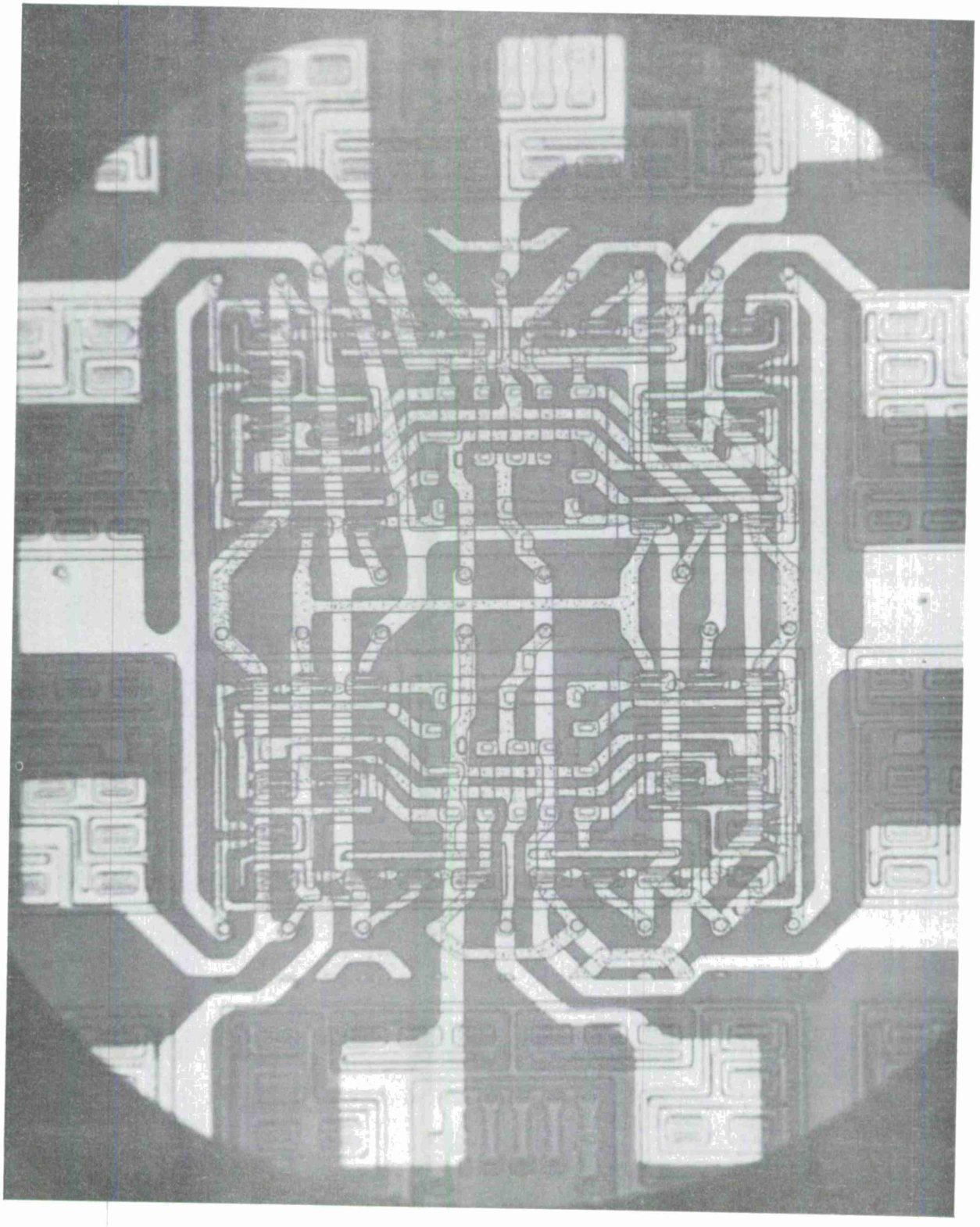


Figure 6. Photomicrograph of 3-Bit Parity Array.

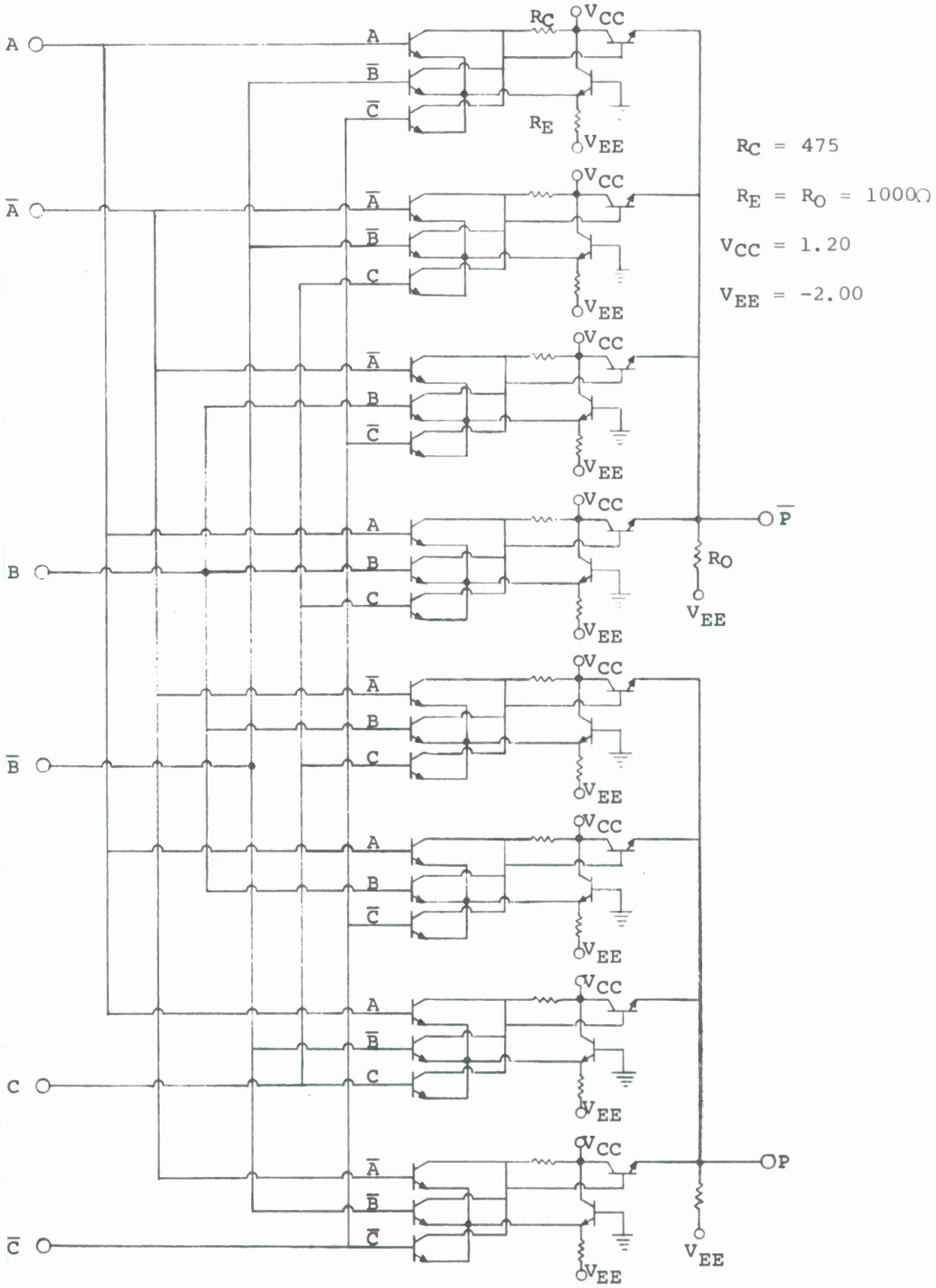
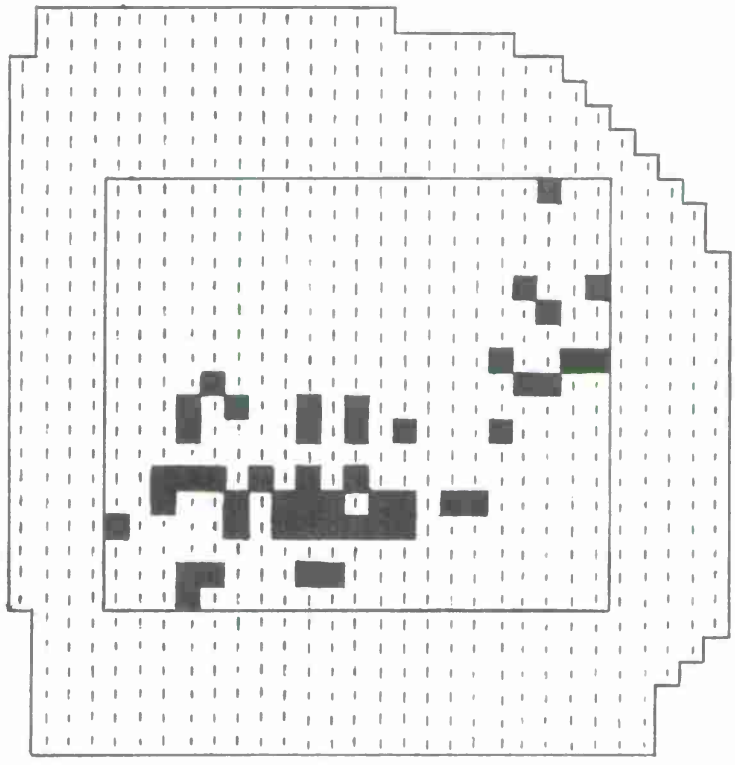


Figure 7. Schematic diagram of 3-Bit Parity Array.

yields. Figures 8, 9 and 10 show die sort maps of 3-Bit Parity Arrays fabricated with the improved technology. Wafer 14A, which had a 5.3% yield, was fabricated using the high-yield microcircuit process, but employed the bimetal (Al-Ni) film for first-level metal. Overall calculated transistor yield was 93% (random defect model.) The remaining three 3-Bit Parity Array wafers in this lot were fabricated with the improved all-aluminum multilevel process. They yielded more than 800 functional arrays at die sort. Overall array yields ranged from 10.7% to 31.6%; overall transistor yields calculated from array yields ranged from 94.6% to 97.1%. In the high yield section of one wafer, #17c, which contained 308 functional arrays, array yield was 63.1% and the calculated transistor yield was 98.8%.

It should be pointed out that some of the 3-Bit Parity Arrays that were described above (wafers 14A and 14D) employed ⟨100⟩ orientation silicon substrates, whereas the remainder employed conventional ⟨111⟩ substrates. Substrates of ⟨100⟩ orientation have been reported to improve the yields of devices (by reportedly allowing more uniform diffusion control and, consequently, finer control of basewidth and collector-to-emitter leakage), but thus far no pronounced yield difference has been apparent between devices fabricated on the two differently oriented substrates.

A group of 20 3-Bit Parity Arrays employing all-aluminum



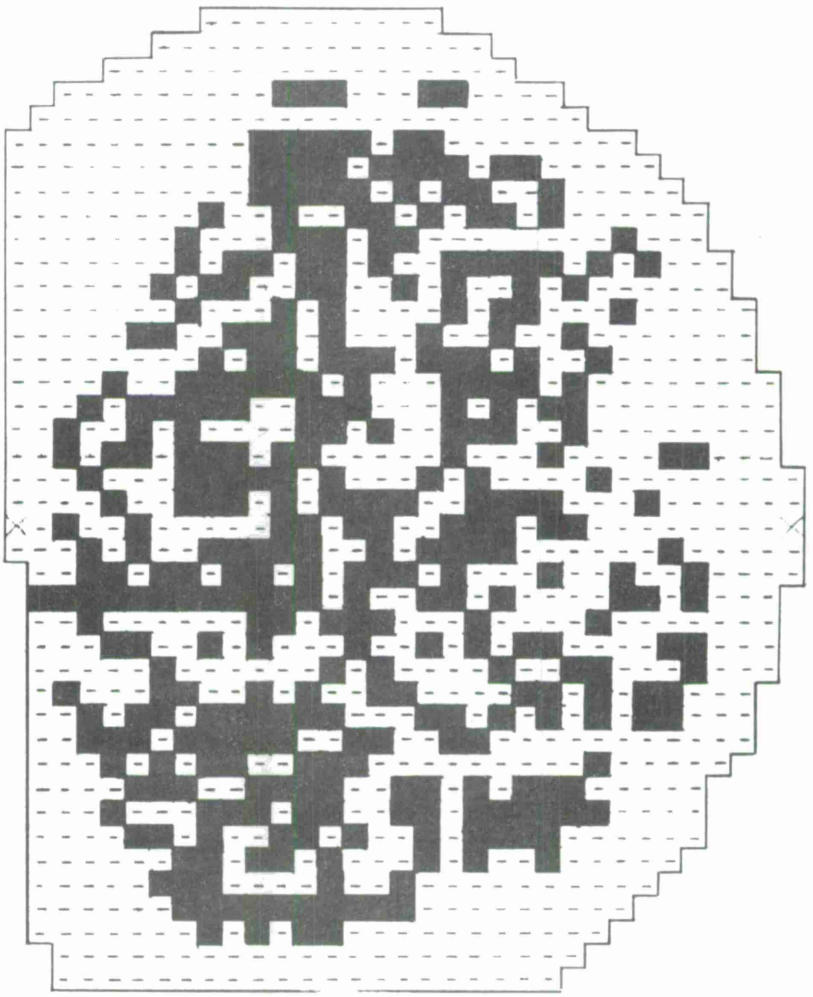
Overall array yield ---------- 5.3%

Array yield in center of wafer ------- 12.4%

Overall calculated transistor yield -- 93.0%

Transistor yield in center of wafer -- 95.0%

Figure 8. Wafer map showing location of functional 3-Bit Parity Arrays on Wafer No. 14A.

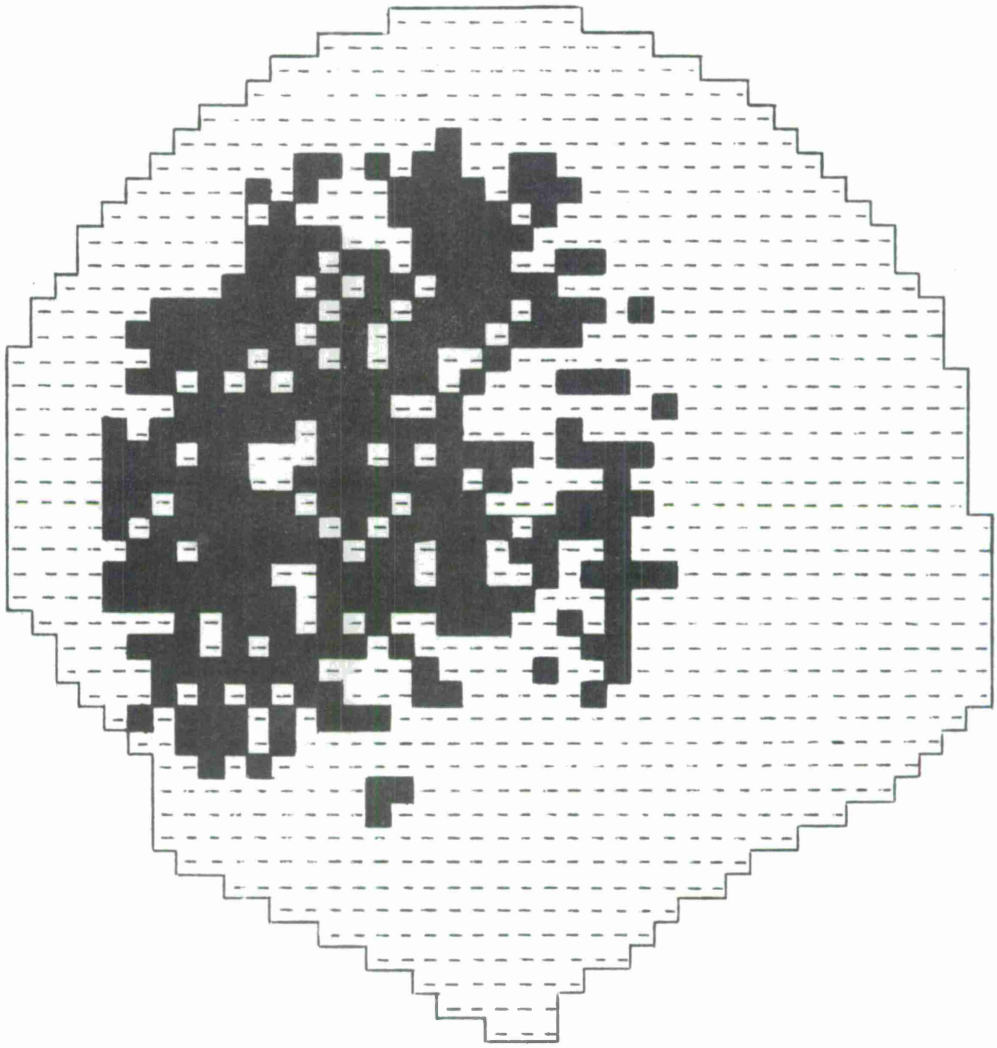


Total number of functional arrays ---- 363

Overall array yield ---------- 31.6%

Overall calculated transistor yield -- 97.1%

Figure 9. Wafer map showing locations of functional 3-Bit Parity Arrays on Wafer #14d.



Total number of functional arrays ---- 314

Overall array yield ---------- 24.8%

Array yield in center of wafer ------- 63.1%

Overall calculated transistor yield -- 96.6%

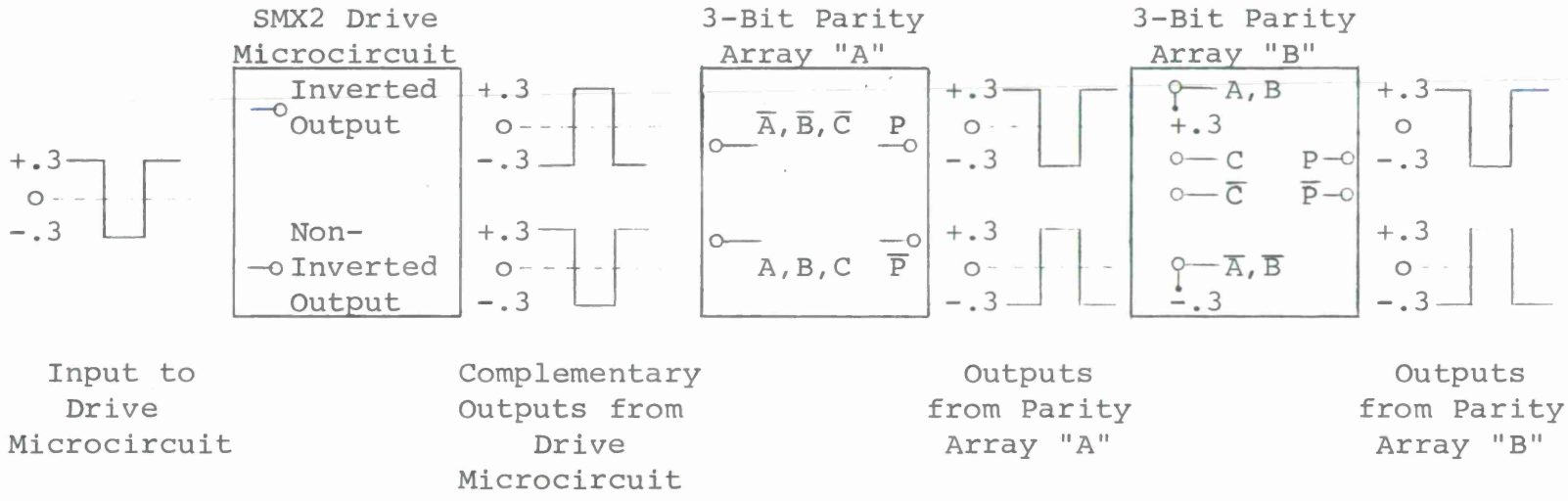
Transistor yield in center of wafer -- 98.8%

Figure 10. Wafer map showing locations of functional 3-Bit Parity Arrays on Wafer #17c.

metalization are being tested for reliability. The tests include thermal shock, back bias-temperature cycling, and operational-temperature sequences. After 250 device hours of temperature cycling between -65°C and 150°C, and 20,000 device hours of back bias-temperature cycling (150°C), there have been no failures.

The switching speed properties of typical 3-Bit Parity Arrays were measured using the test arrangement indicated in Figure 11, which permits the determination of array propagation delay time under two simulated system conditions. Array A simulates a case in which all 24 of the array input transistors are being switched, while the array is driving a fanout of four. Array B simulates the case in which 8 of the array input transistors are being switched, while the array has no circuit fanout, driving only the capacitance of the test probe (1.8 pF.)

The average propagation delay for arrays tested in Position A was 1.48 to 1.53 ns. Propagation delay for arrays in Position B was 0.91 to 1.00 ns. The microcircuit employed to drive a 3-Bit Array A is a high speed ECL gate (the SMX2 developed on an earlier program) having a raw delay of <0.4 ns and a propagation delay of 0.90 ns, when driving a fanout of 12 as when driving Array A. Average power dissipated by the 8-gate, 3-Bit Parity Arrays was 57 mW. It should be noted that the propagation delay of the 3-Bit Parity Array could have been made lower at the expense of



	Average Measured* Propagation Delay	Operating Conditions	
		Fan-In	Fan-Out
SMX2 Drive Microcircuit	.90 nsec.	1	12
3-Bit Parity Array "A"	1.50 nsec.	12	4
3-Bit Parity Array "B"	.95 nsec.	4	0**

* These measurements include the effect of package and stray capacitances.

** Parity Array "B" drives test probe capacitance of 1.8 pF.

Figure 11. Illustration of test method used to measure propagation delay time through 3-Bit Parity Arrays, and chart of propagation delays.

power dissipation. Array resistors were, however, designed to maintain the relatively low power dissipation described above.

3.1.2 Read-Only Memory Array (ROM)

The Read-Only Memory chip is an array of 256 transistors interconnected in the emitter follower mode, by two levels of metalization. (Emitter follower resistors are not included on the chip.) This memory is capable of storing 16 words at 16 bits per word. Following are some significant features of the ROM:

1. The array layout was designed using the computer-aided drafting (CAD) techniques described in subsection [redacted]. This effort demonstrated the unique capability of computer aid to rapidly and accurately effect layout design of repetitious microcircuit features, such as the 16 x 16 transistor matrix of the ROM chip. Figure 12 shows a complete ROM chip. Figure 13 illustrates schematically the ROM chip.
2. The entire active area of the array chip occupies only 256 $mils^2$ (1 mil^2 per transistor, including interconnections.) The transistors are 0.1-mil geometry devices, with emitter and base contact cuts which are 0.1 x 0.3 mils, and with a base area of 0.25 $mils^2$.

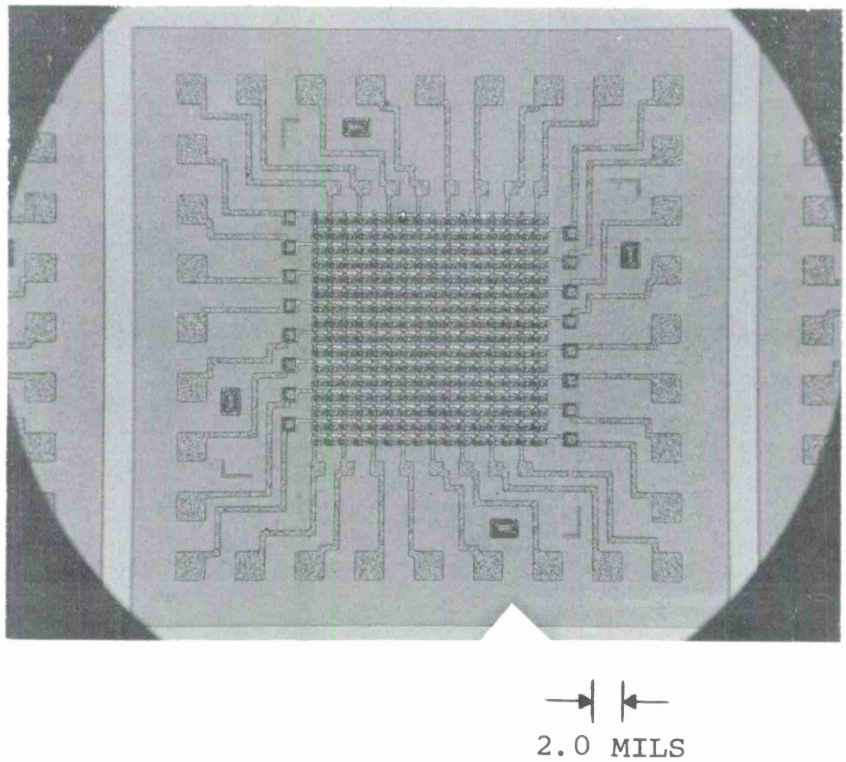


Figure 12. Photomicrograph of 256-Bit Read Only Memory chip.

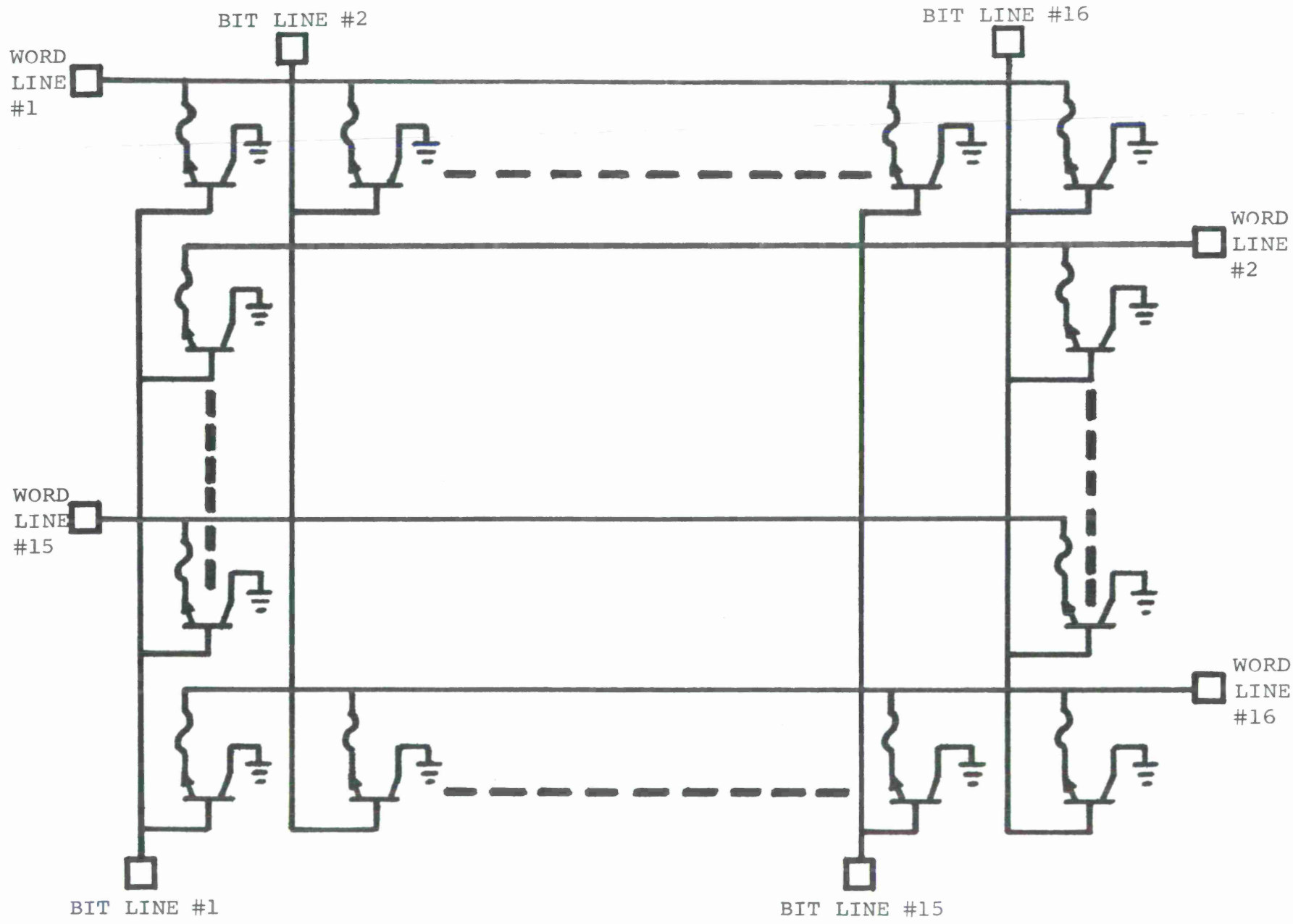


Figure 13. Schematic diagram of Read Only Memory Array.

3. The ROM array was designed to be programmable in chip or package form through selective fusing. Narrow (0.1 mil) emitter metalization fingers were designed to act as fuses which could, in principle, be electrically "burned open" by electromigration effects induced by passage of high current densities through the narrow aluminum fingers. Metal contacts to the base contact stripes were designed to pass similar currents without being affected by electromigration. Figure 14 illustrates the transistor geometries including the fuses.
4. Interconnection of the ROM requires two levels of metalization and 1 insulator via per transistor; vias are 0.2 x 0.2 mil^2. The ROM chip, because it contains 256 vias, has been an excellent vehicle for characterizing the improved process for photoengraving of vias in terms of its effectiveness to produce large numbers of small-area, low-resistance vias.

Die sort evaluations of the first two ROM Array wafers to be produced indicated a yield of four perfect ROM Arrays; this represents a yield of ≈0.3%. No via problems were encountered in these arrays. The predominant failure mode encountered was metalization shorts across the narrow (0.1-mil) emitter-base spacing. By optimizing the metal photoengraving process, on sub-

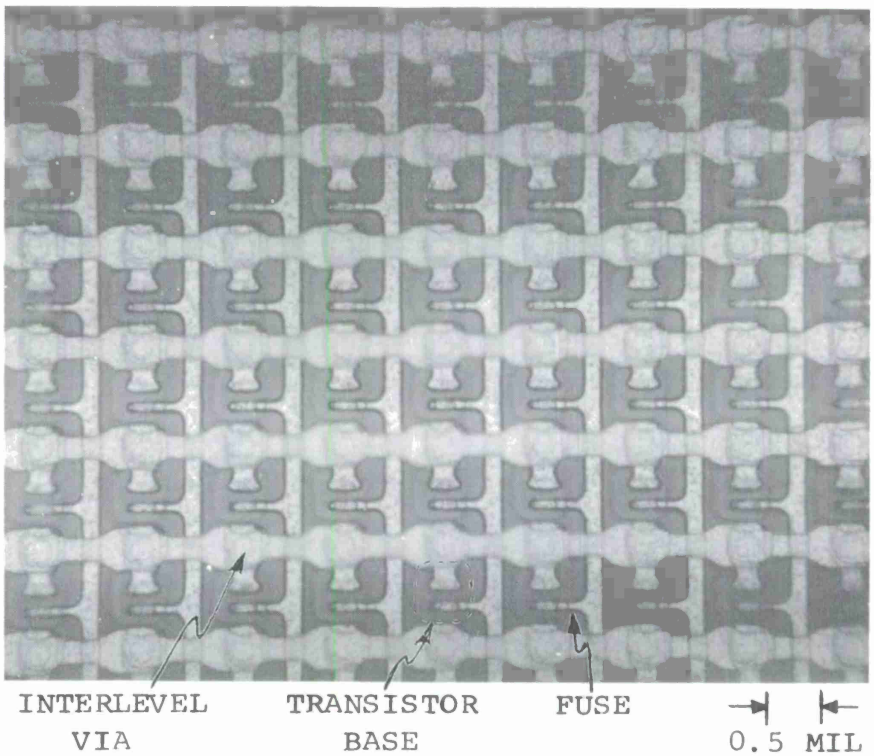


Figure 14. High magnification photomicrograph of 256-Bit Read Only Memory chip.

sequent ROM wafers, die sort yields as high as 37% were realized. Packaged devices were shipped to and tested by Lincoln Laboratories.

An interesting fundamental design restriction was uncovered during evaluation of ROM Memory chips. As was described above, the ROM was designed to be programmed by "burning open," through induced electromigration, selected 0.1-mil emitter fingers. It was found, however, that electromigration in the first-level metal fingers was retarded by the presence of the vapox* insulator. The net effect was that during the attempted fusing process, fields and temperatures became sufficiently high between the emitter and base metalization (spacing = 0.1 mil) that electromigration took place between these metal stripes, before electromigration occurred in the fuses. As a result, junction shorts rather than opened fuses were created. This suggests that future designs of fusable memory arrays should incorporate fuses in the top level rather than bottom level interconnection scheme.

3.2 THREE-LEVEL ARRAYS

During the last quarter of this program, efforts were concentrated on fabricating three-level arrays, employing the yield improving technologies, which were developed in the two-level arrays during the previous quarter. The vehicles employed in

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* Vapox = vapor deposited SiO_2.

this effort included the Parity Check Arrays and the Functional Multiplier Array. (See paragraph 1.3.2 for details.) Schematic diagrams and photomicrographs of each are shown in Figures 15 through 19. A number of wafers of each type were fabricated, tested and analyzed. None of the three-level arrays were found to function completely, although some functioned in part. A detailed analysis of all array types fabricated and of the processes employed, revealed the following information:

1. Our high-yield microcircuit process has resulted in transistor yields which were certainly adequate to successfully fabricate functional samples of all of the three-level arrays that were attempted. Evidence of this is obtainable from a number of sources. Calculations were made to determine what minimum transistor yield was required to obtain one array per wafer of each of the types of arrays in question, assuming a random defect model. The minimum transistor yield required was found to be 95% for the Functional Multiplier; 96% for the 9-Bit Parity Array; and 99.7% for the 27-Bit Parity Array. Randomly sampled transistor yields in actual three-level array wafers (tested at the point of first-level metal) typically ranged between 93 and 98%. The average yield is even higher in the central higher

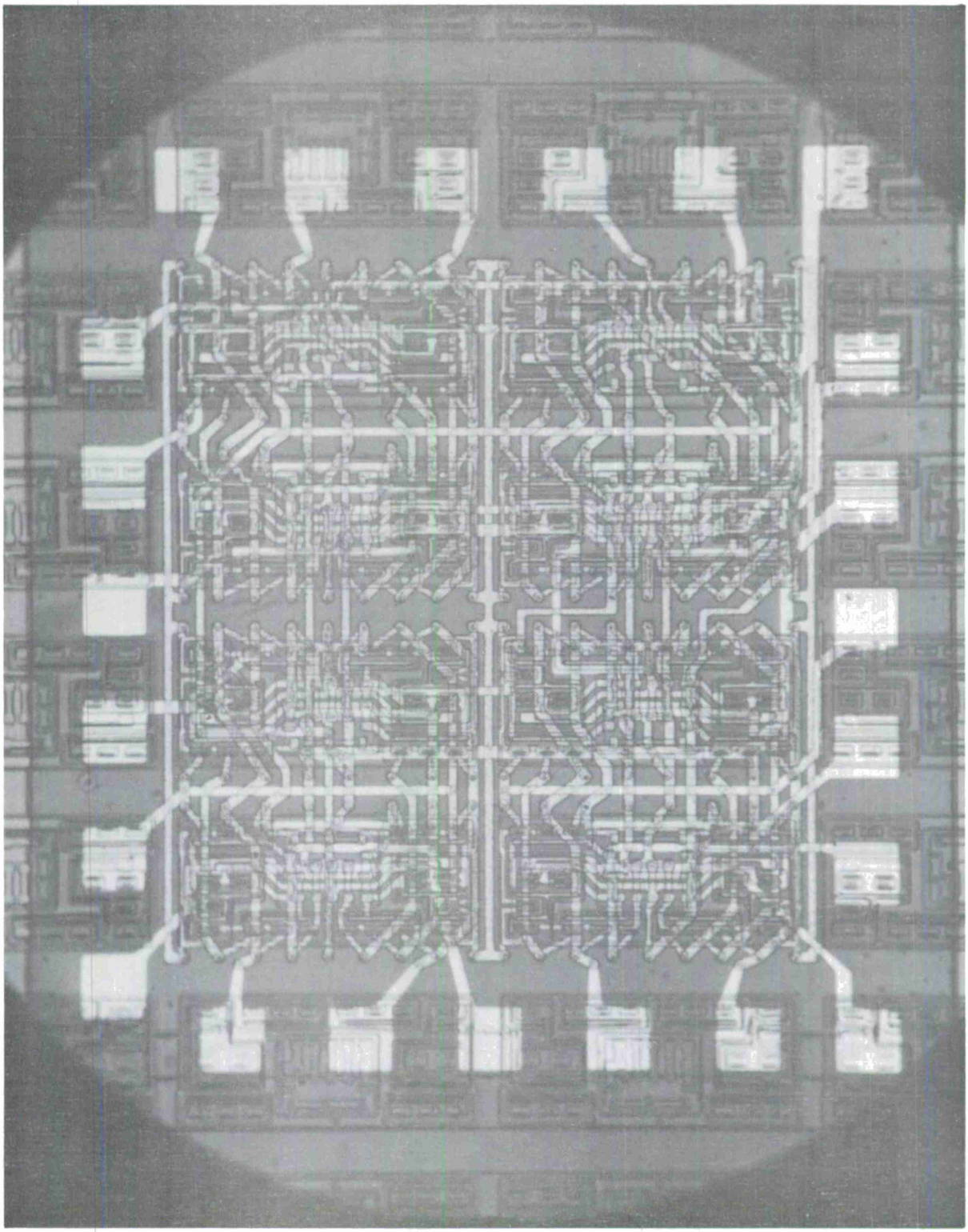


Figure 15. Photomicrograh of 9-Bit Parity Array.

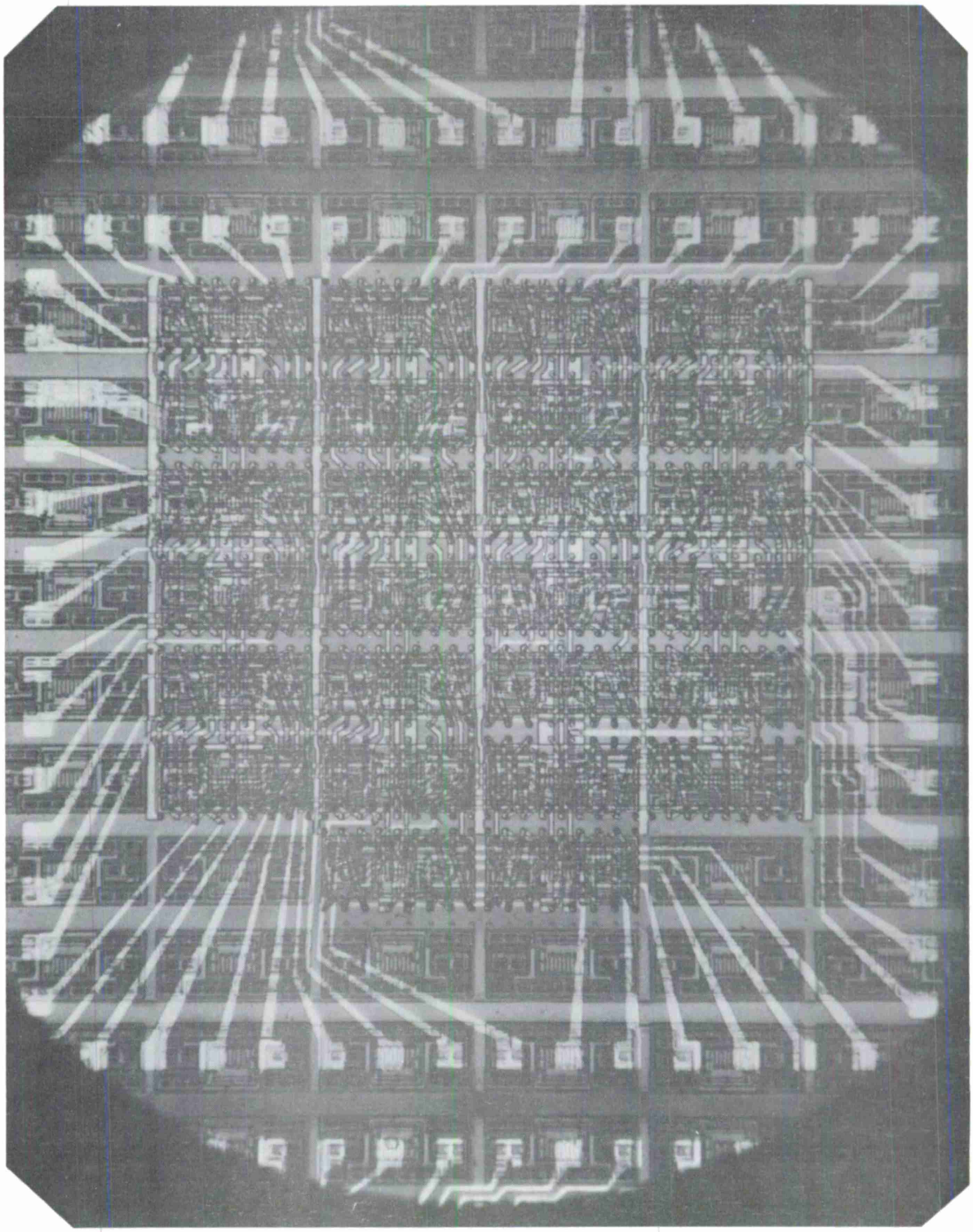
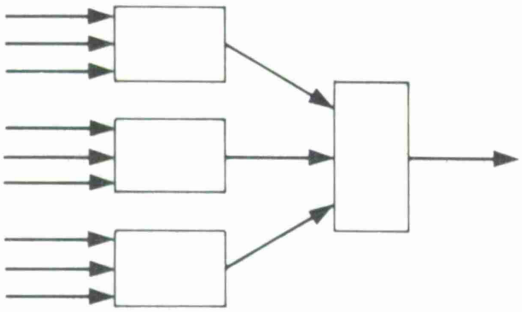
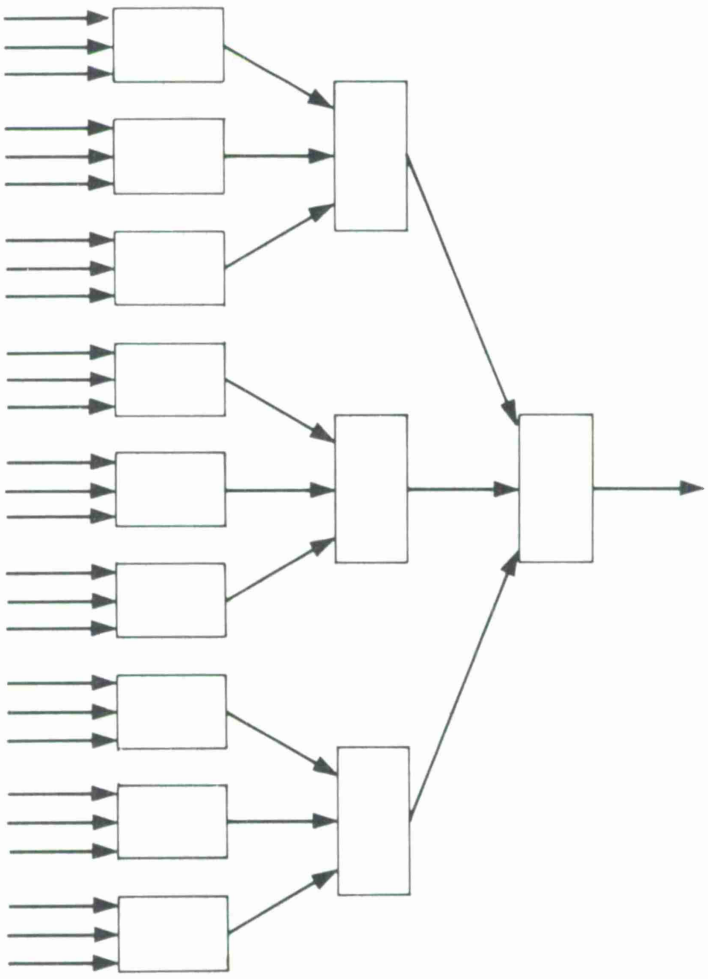


Figure 16. Photomicrograph of 27-Bit Parity Array.



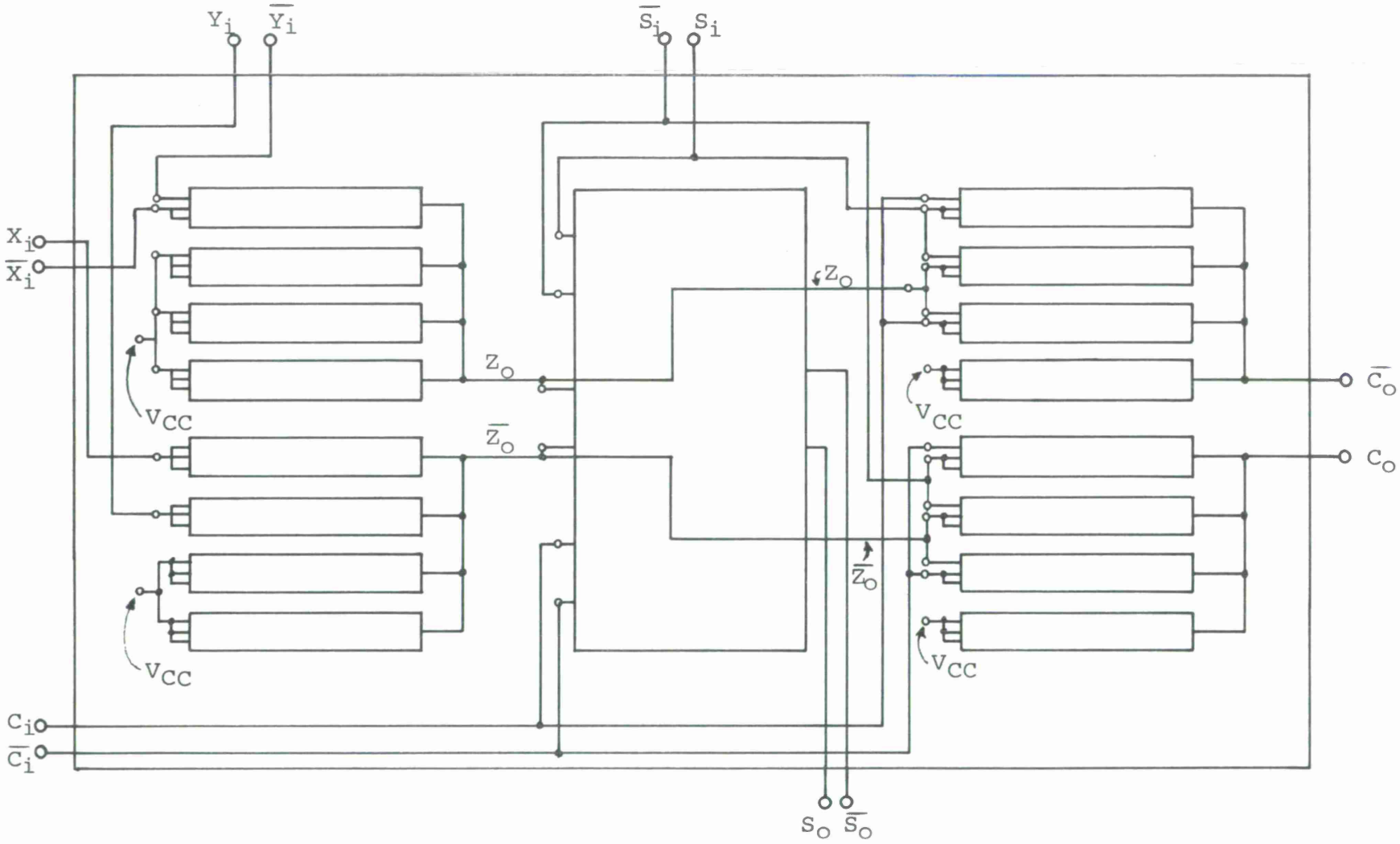
a. 9-Bit Parity Checker (160 transistors and 72 resistors -- a total of 232 components; power dissipation = 144 mW).



b. 27-Bit Parity Checker (520 transistors and 234 resistors -- a total of 754 components; power dissipation = 468 mW).

NOTE: Each rectangle represents a 3-bit parity circuit.

Figure 17. Functional block diagrams showing formation of 9-Bit and 27-Bit Parity Checkers by extensions of the 3-Bit Parity Circuit.



Note: This diagram illustrates the implementation of the circuitry of three 3-Bit Parity Cells to form the Multiplier. The small rectangles represent the basic 3-input gates of the parity cell; the large rectangle represents a 3-Bit Parity Circuit.

Figure 18. Schematic diagram of 1 x 1 Functional Multiplier.

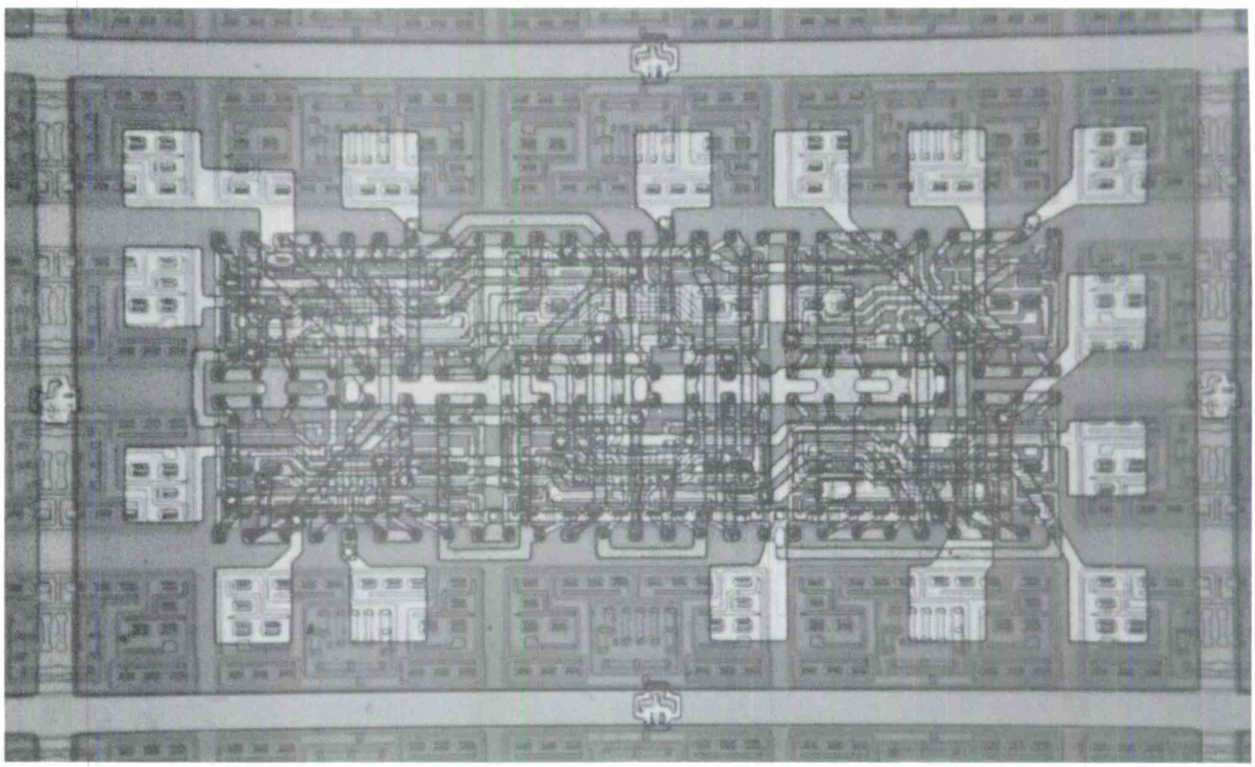


Figure 19. 1 x 1 Functional Multiplier Array.

yield portions of wafers. This was verified by calculations of transistor yields on 3-Bit Parity wafers, based on die sort array yields. As an example, illustrated in Figure 10, transistor yields in some portions of wafers ran in excess of 98%. (Inasmuch as all of the Parity Checker Arrays and the Functional Multiplier Array employ the same basic microcircuit cell, shown in Figure 20, extrapolations from data obtained from the bilevel 3-Bit Parity Arrays are valid.)

The adequacy of transistor yields obtainable with our process is further attested to by examining die sort maps of 3-Bit Parity Arrays, such as that shown in Figures 9 and 10. Inasmuch as the Functional Multiplier Array, 9-Bit Parity Array and 27-Bit Parity Array are composed of matrices of 1 x 3, 2 x 2 and 4 x 3 plus 1 3-Bit Parity Arrays, it can be shown that wafer 17c potentially contained 40 Functional Multiplier Arrays, 24 9-Bit Parity Arrays, and two 27-Bit Parity Arrays, assuming that the componentry of these arrays were 100% effectively interconnected. Figure 21 illustrates the possible locations of the 24 9-Bit Parity Arrays.

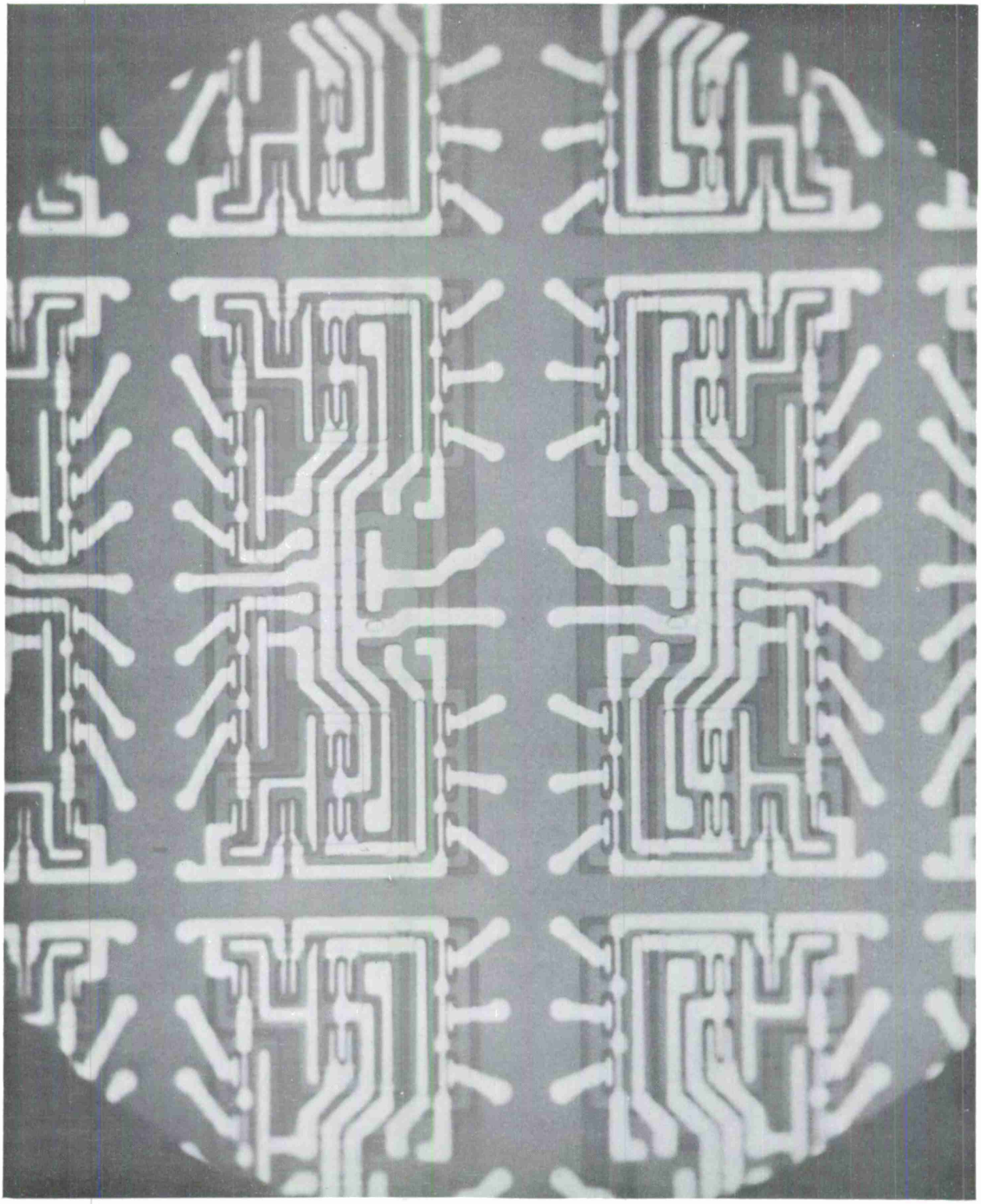


Figure 20. Basic cell pattern for parity arrays.

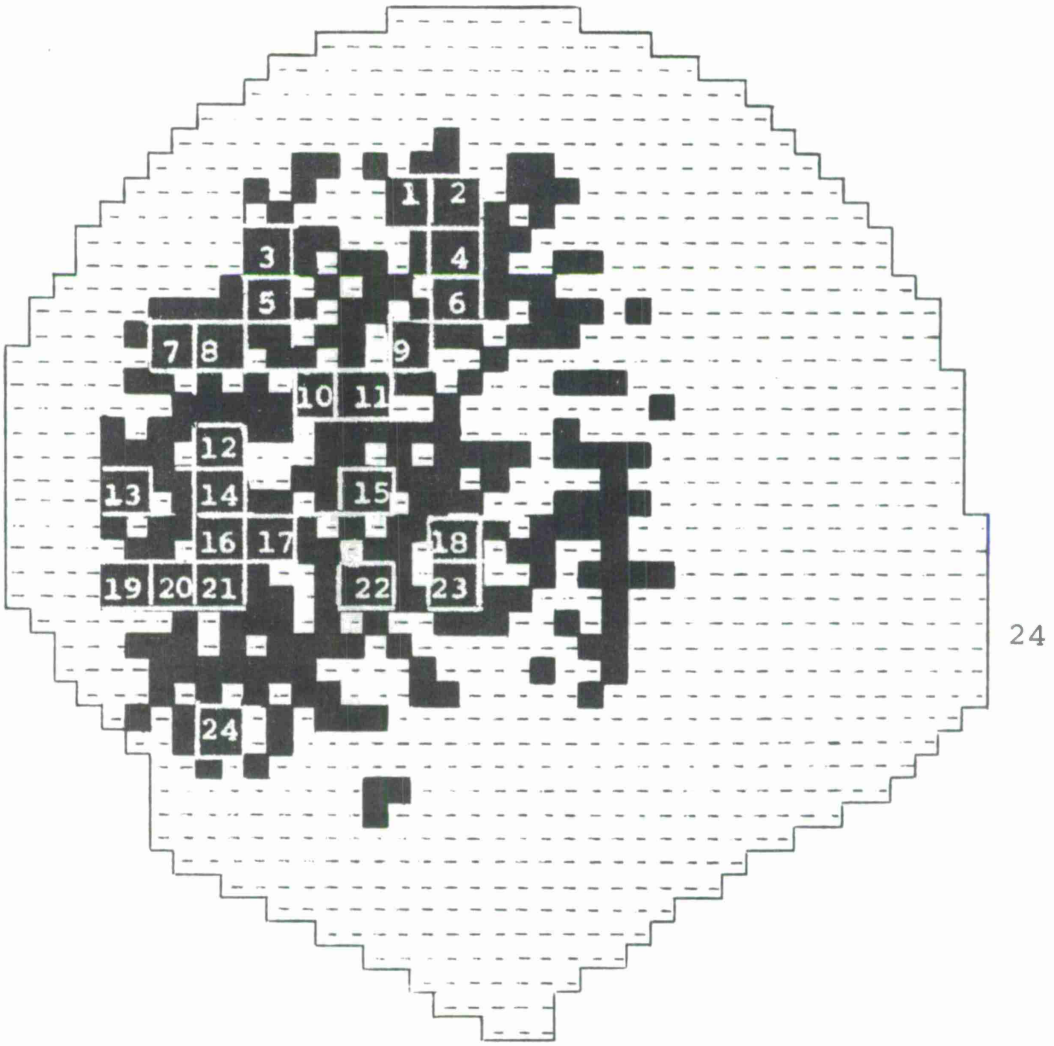


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Figure 21. Wafer map showing locations of 24 potential 9-Bit Parity Arrays on Wafer #17c.

2. The quality of the deposited vapox insulating employed in the three-level arrays was not a factor preventing their proper functioning. Calculations indicate that less than 3% of 27-Bit Arrays, the most complicated of the three-level arrays (possessing some 400 $mils^2$ of conductor crossover), were affected by insulator pinholes. Only 1% or less of the other arrays (9-Bit Parity Array and FM Array) were affected by insulator pinholes.

3. The overwhelming failure mode in all of the three-level arrays was high resistance and electrical discontinuity through vias in the second-level insulator, i.e., between second- and third-level conducting films. Vias in the first-level insulator did not have this problem even though first-level vias were designed to be slightly smaller in cross-section - the minimum cross-sectional area of first-level via was typically 0.047 mil^2, whereas the minimum cross-sectional area of second-level vias was typically 0.07 mil^2. Detailed analyses of the problem led to the determination that only certain vias had the "open" problem and that the affected vias were located on irregular substrate topography, i.e., the vias were located over discontinuities in the substrate surface

caused by conductor steps, steps in the silicon, or oxide steps. The presence of irregular topography beneath the small area vias affects the vias because it affects the growth pattern of the vapox and because it affects photoengraving of the vias.

This problem can be solved by one of two methods:

a. Locate second level vias only on flat topography.

b. Enlarge vias which are located over irregular topography.

However, these improvements could not be accomplished before the end of the program.

IV - ARRAY PACKAGING

For the most part, the arrays developed thus far have been packaged using flatpacks manufactured by Philco-Ford. The 3-Bit Parity Array, 9-Bit Parity Array and Functional Multiplier Array are packaged in Philco-Ford standard line 14-, 24- and 16-lead packages, respectively. The 27-Bit Parity Array required the development of a 60-lead flatpack. This package, shown in Figure 22, was fabricated in limited quantities to package and evaluate the 27-Bit Parity Array. A commercial package developed for this application would not necessarily have the same configuration. Final testing of arrays in the 60-lead package is accomplished by soldering the package leads into an appropriately designed printed circuit board, shown in Figure 23, which can be connected to the testing apparatus by means of commercially available sockets.

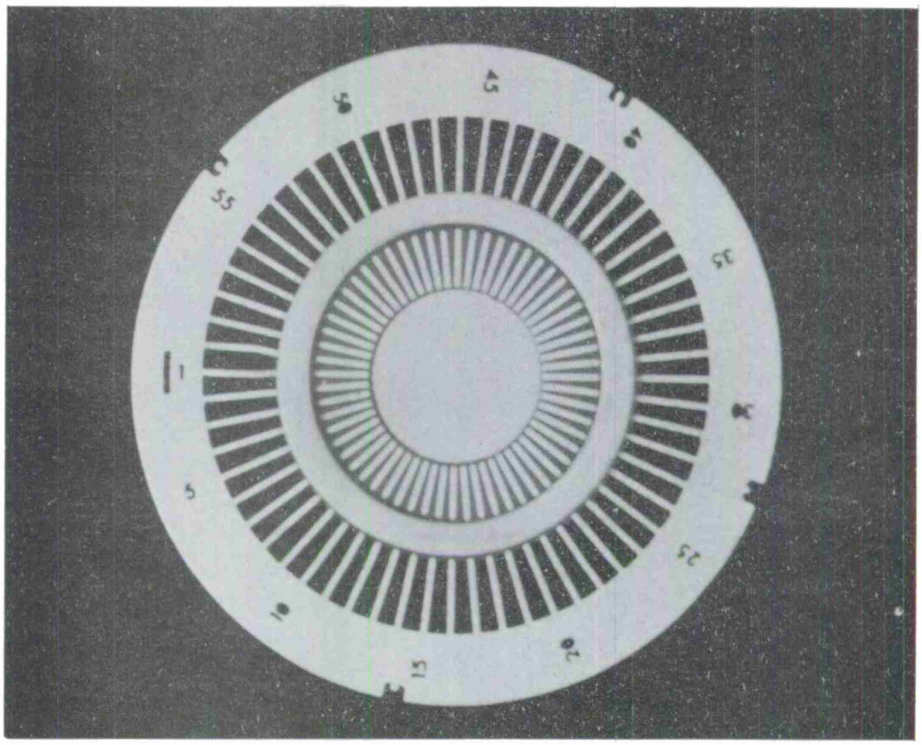


Figure 22. Sixty-lead experimental package.

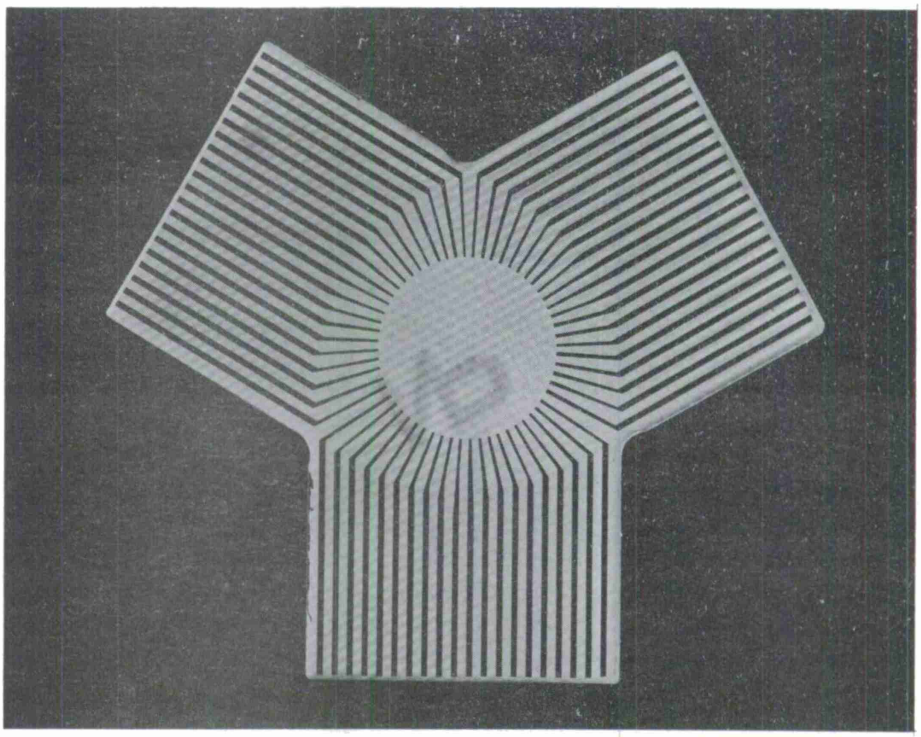


Figure 23. Experimental printed circuit test board for 60-lead package shown in Figure 22.

V - ARRAY EVALUATION AND FAILURE ANALYSIS

5.1 TESTING

Exhaustive testing of complex arrays is a very difficult, expensive and time consuming task, in terms of both the equipment required and the time required to design test sequences. On this program, die sort testing has been done with both standard and special probes developed by Philco-Ford in conjunction with a Functional Tester which was designed and provided by Lincoln Laboratory. The Array Functional Tester shown in Figure 24 can test the Parity Arrays and the Functional Multiplier. The test sequences, for example, test all gates for all possible combinations of inputs in the 3-Bit Parity Array, and exercises at least once each gate in the 9- and 27-Bit Parity Arrays.

Due to the large number of terminal pads on arrays of the complexity of the 9- and 27-Bit Parity Arrays, special probe assemblies were required for die sort testing. Figure 25 shows the probe board assembly developed by Philco-Ford for testing the 27-Bit Parity Array. This probe is capable of contacting fifty-nine 2.5 x 2.5 mil pads with 2.5 mil spacing. The probes are fixed-positioned and individually spring loaded.

Testing of the Parity Arrays after packaging has been conducted using the Array Functional Tester for low-frequency measurements and specially designed test sets for high-speed measurements.

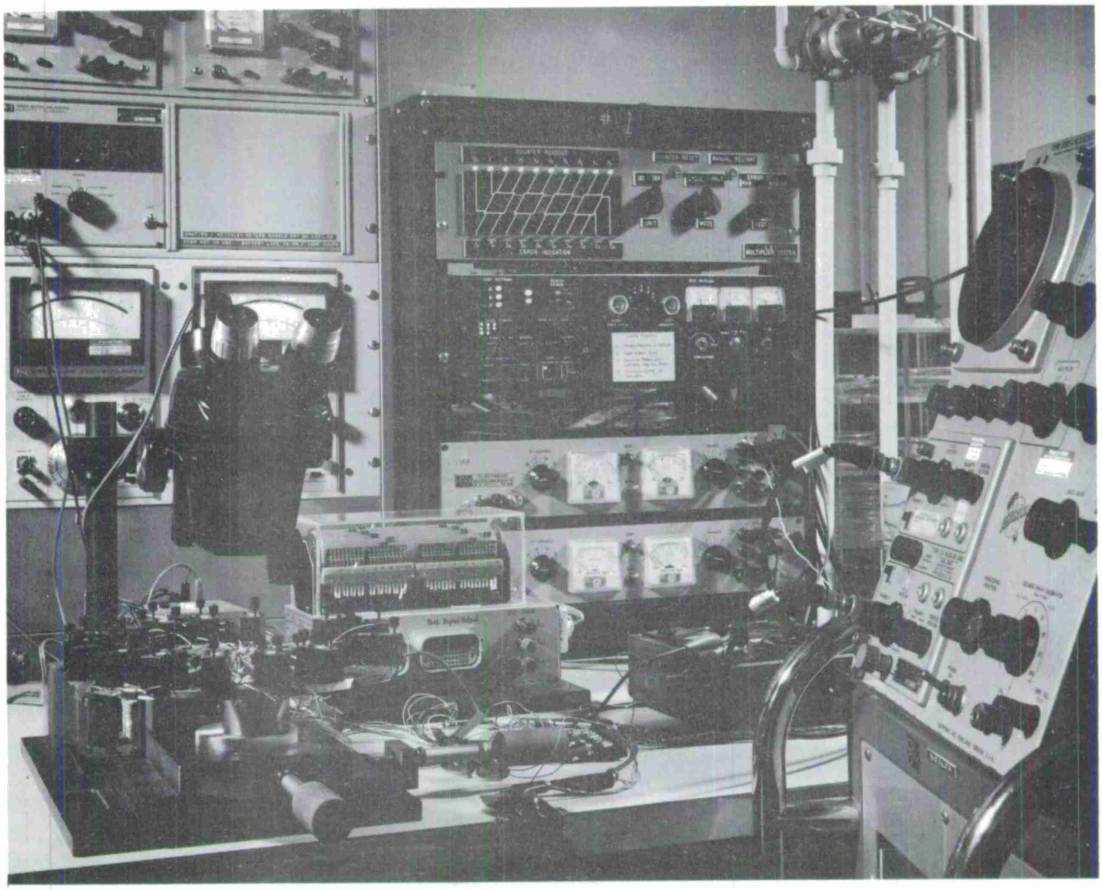


Figure 24. Array functional tester.

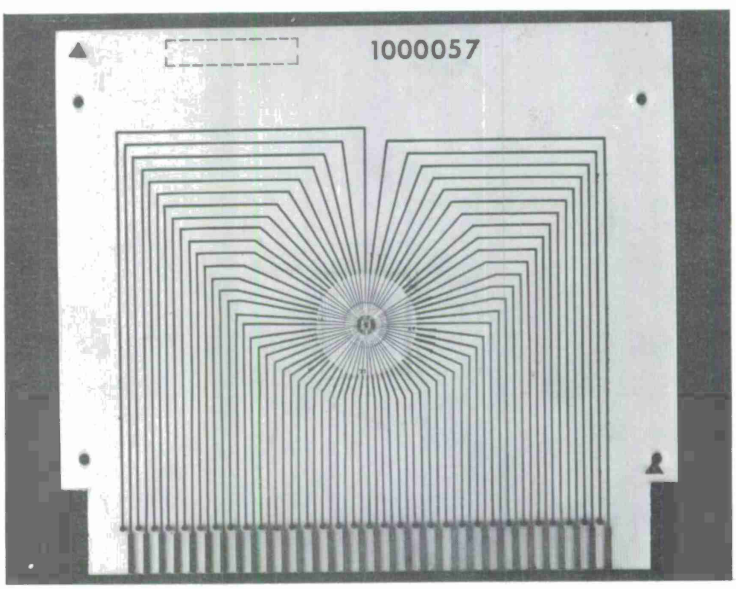
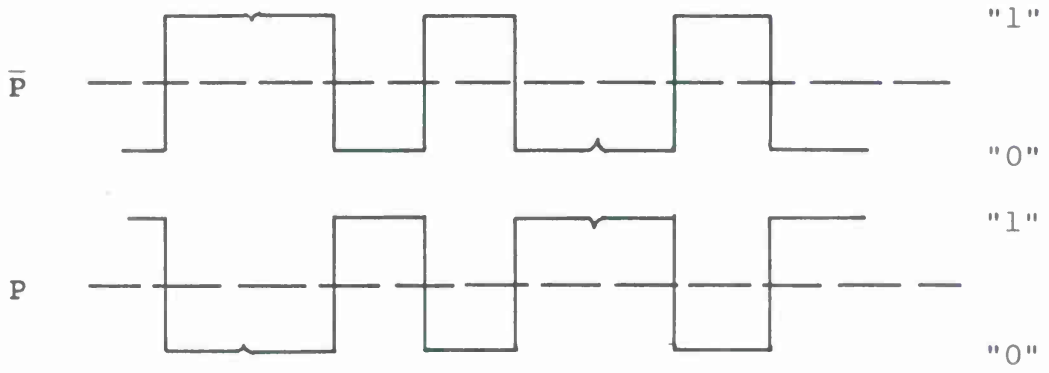


Figure 25. Fifty-nine pin micro test probe.

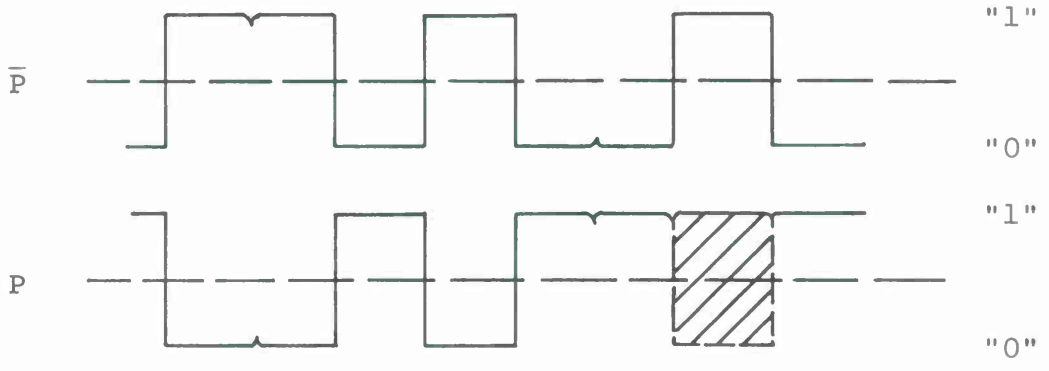
5.2 FAILURE ANALYSIS

Array failure analysis was initially accomplished solely by a 2-point pad probing technique. However, this technique was later supplemented by a technique which obtains analytic information from the output waveforms displayed by the Array Functional Tester on a sampling scope. By using the combination of the two techniques it has been possible, in many cases on 3-Bit Parity Arrays, to pinpoint, in particular components or sections of the arrays, failures due to opens or shorts. Open vias can also be located using these techniques. As an example, Figure 26a shows the output waveform of a properly functioning 3-Bit Parity Array. The waveform of Figure 26b signifies that any one of four specific transistors has an open lead or a defective emitter-base junction. These techniques have been valuable in analyzing 3-Bit Parity Arrays; similar analyses became more difficult on the more complex arrays.

Failure analyses can also be performed by probe testing the internal interconnections of the arrays to some degree. Even though this technique is somewhat restricted, due to the fact that the metalization lines on the first and second levels cannot be probed without destroying (by etching away) the overlying insulator and metal, the technique has been valuable in analyzing failures of both two- and three-level arrays.



a. Proper output waveforms for given sequence of test inputs which completely exercise the 3-Bit Parity Array.



b. Waveforms which are obtained, for example, when a specific single input transistor has an electrical open or a degraded emitter-base diode.

Note: "1" = +0.3 V
"0" = -0.3 V

Figure 26. Output waveforms of properly functioning 3-Bit Parity Array (a), and of malfunctioning 3-Bit Parity Array (b).

VI - SUBSYSTEMS ASSEMBLY

To achieve the program goal of developing a compatible assembly technique for interconnecting high-speed microcircuit array chips into a subsystem, through means other than conventional packaging and wiring, a face-down bonded version of the 9-Bit Parity Checker has been developed.

6.1 FACE-DOWN BONDING

During the third quarter, functional face-down bonded 9-Bit Parity Checker subsystems were assembled. The 9-Bit Parity Checker subsystem consists of four 3-Bit Parity Array chips (circuit chips) face-down bonded onto a silicon interconnection substrate (wafer-chip). The wafer-chip is prefabricated with one level of aluminum interconnections and with electroplated gold interconnect pedestals. Figure 27 illustrates the 9-Bit subsystem interconnect chip and the constituent 3-Bit circuit chips. Figure 28 shows an assembled subsystem. Face-down chip bonding was performed with thermocompression techniques, the heat energy being provided by a constant temperature heat column upon which the assembly is performed. There are 48 gold interconnection pedestals in the 9-Bit Parity Checker subsystem. The pedestals are 2.0 mils in diameter and 9 to 10 microns high.

The face-down bonding was performed with the custom-built commercial bonder shown in Figure 29. Alignment accuracy was

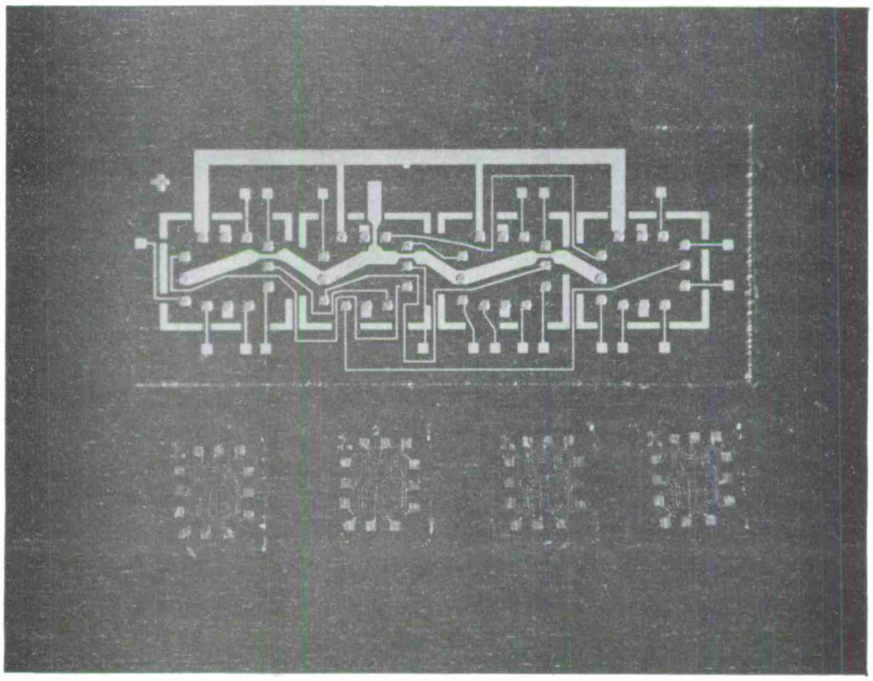


Figure 27. Components (3-bit parity circuit chips and interconnection wafer-chip) for face-down bonding assembly of a 9-Bit Parity Subsystem.

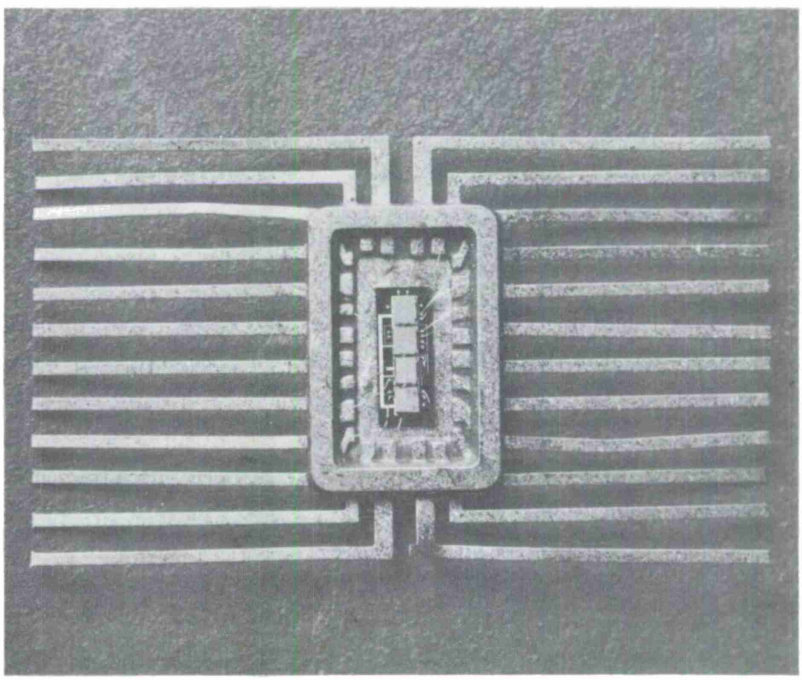


Figure 28. Photograph of a face-down bonded 9-Bit Parity Checker subsystem.

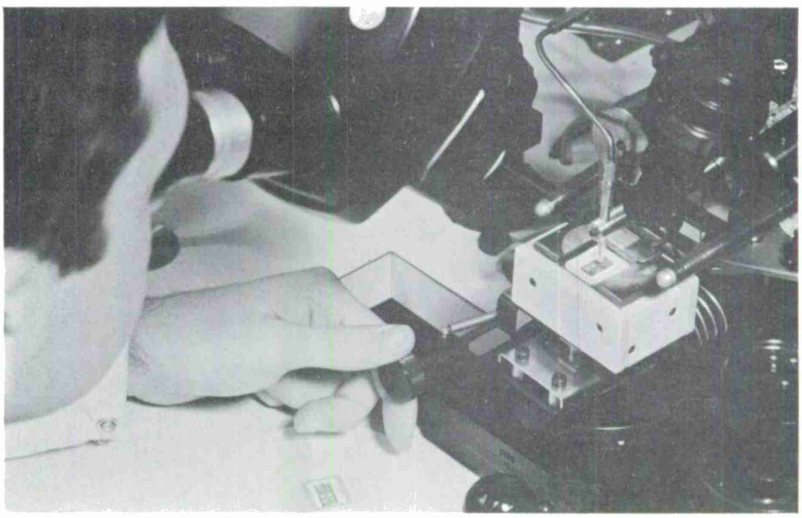


Figure 29. Face-down bonding equipment.

specified to be within ±0.25 mil; however, to obtain optimum bonding performance, it was necessary to develop an improved chip-to-chip alignment fixture and a vacuum chuck which permits automatic leveling of the circuit chip relative to the wafer-chip during the bonding sequence.

6.2 ADVANTAGES OF FACE-DOWN BONDING

The face-down bonding concept of subassembly is versatile in a number of ways:

1. The wafer-chip can be completely passive, that is it can be an oxidized silicon substrate having a metalization pattern appropriately processed with Au-plated contact bumps to interconnect various completed microcircuit chips which are face-down bonded onto it.
2. In addition to interconnecting microcircuit chips by means of a metalization pattern, the wafer-chip can be utilized as a power buss.
3. The wafer-chip interconnection pattern can be a multi-level structure, with the wafer-chip substrate being used as a power buss, lending still another option.

The substrate for the 9-Bit Parity Checker subsystem, besides serving as an interconnection chip, also serves as a ground reference power buss.

To determine the improvement in subsystem speed that results from assembling the 9-Bit Parity Checker in a single package via face-down bonding, the propagation delay through a 9-Bit Parity Checker thus assembled was compared with the propagation delay through a 9-Bit Parity Check, assembled by interwiring discretely packaged 3-Bit Parity Checker Arrays. The per-stage propagation delay was 11% lower on the face-down bonded system, measuring 1.22 ns, compared to 1.37 ns for the wired version.

6.3 THERMAL ANALYSIS OF THE FACE-DOWN BONDING SUBSYSTEMS

Subsystems assembled by face-down bonding can be expected to have greater thermal problems than subsystems assembled by conventional techniques. This occurs because the face down-bonded active chips, being thermally separated from the package by the bumps and the interconnection chip, have a higher thermal resistance to the package, than would the same active chips bonded conventionally in the same package. Figure 30 illustrates the two cases. To study the thermal problem, thermal analysis was made of the 9-Bit Parity Checker Subsystem.

Taking into account the thermal resistance contributions in the active chip itself, in the bumps and in the interconnection chip, it was calculated that the thermal resistance from each active chip to the package was approximately 60°C/watt. This figure is slightly high in that in calculating the resistance

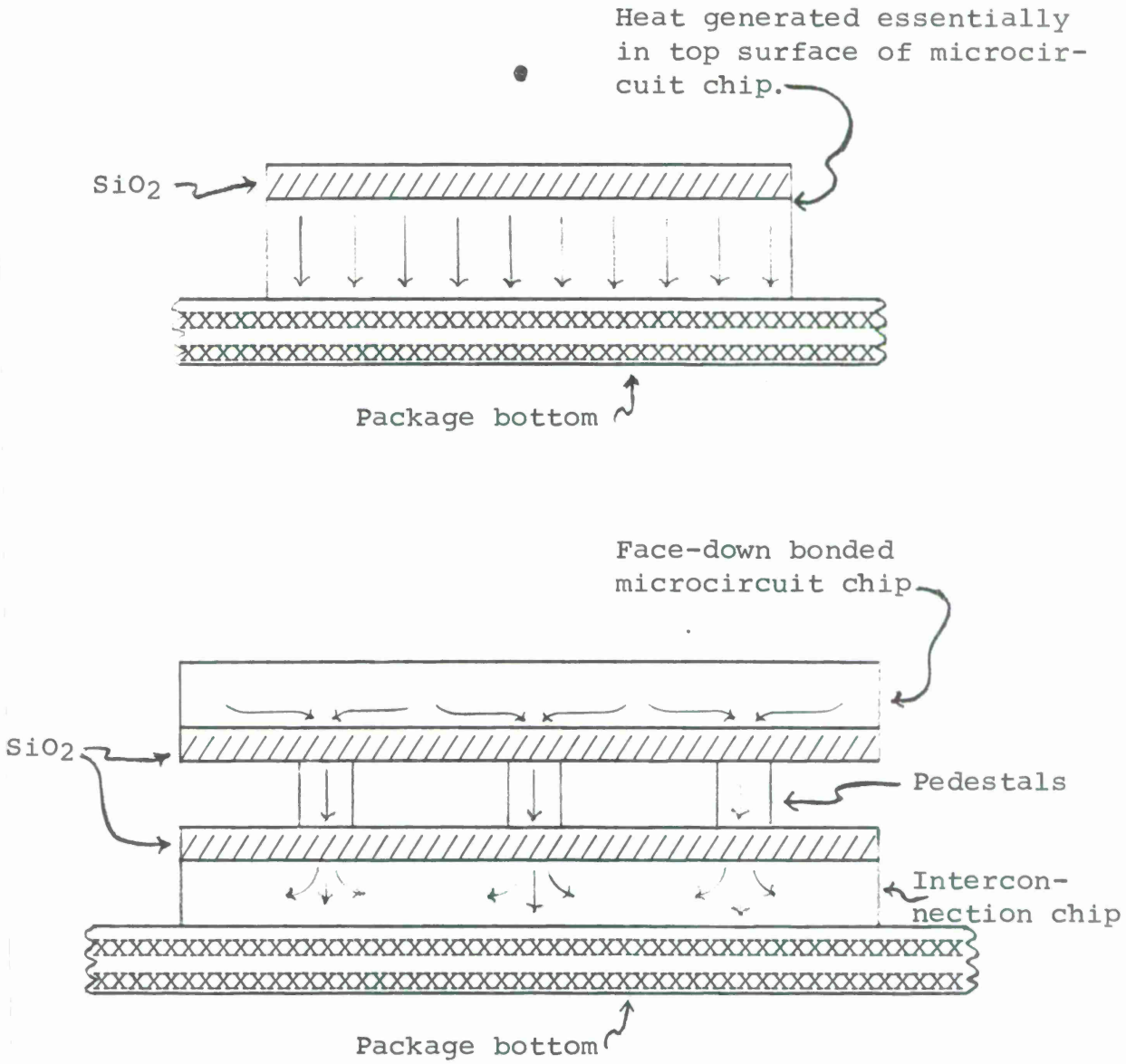


Figure 30. Schematic diagram of heat flow to package (upper) in a conventionally packaged microcircuit and (lower) in a face-down bonded system which utilizes a silicon interconnection chip.

contribution from the active chip itself, it was assumed that all the chip power was dissipated at the center of the chip. The actual thermal properties of an operating 9-Bit Subsystem were determined using infrared scanning techniques. It was found that the thermal resistance, junction to package, of an operational face-down bonded 9-Bit Parity Checker subsystem was 42°C/watt, with approximately 35.5°C/watt directly attributable to the face-down bonded structure. (Thermal resistance to substrate of the 3-Bit Parity Array chip is approximately 6.5°C/watt.) The The thermal resistance to ambient of the package used was 104°C/watt. In all cases, measurements were made to a room temperature, static air ambient.

The following comments are made concerning the thermal properties of face-down bonded subsystems.

1. Since the 9-Bit Parity subsystem dissipates only 230 mW, neither the junction temperature rise above ambient during operation, 34°C, nor the contribution due to face-down bonded structure, 10°C, were high enough to deleteriously affect subsystem performance.
2. However, in subsystems where large circuit chips containing two and perhaps three levels of metalization (and, consequently, several levels of insulator to add thermal resistance between the circuit chip and the actual bump)

dissipating higher power, are used, the temperature increase can become significant in face-down bonded systems. It is difficult to place any limit on the power level of a chip of any given size that is tolerable, unless the chip configuration is known. Such factors as the number and size of pads, the number and size of bumps that will be used, the actual ambient temperature, and the thermal resistance of package to ambient all play interrelating roles in this determination, and must be evaluated for each case.

3. As was the case for the 9-Bit Parity Checker Subsystem, the thermal resistance of the package-to-ambient can be a major contributor to junction-to-ambient thermal resistance. This, of course, can be lowered by heat sinking in typical ways, such as using metal sinks, forced air or forced liquid ambients. Heat sinking can also be applied to the back side of the circuit chip to further lower the thermal resistance of the whole system.

VII - NEW MICROCIRCUITS

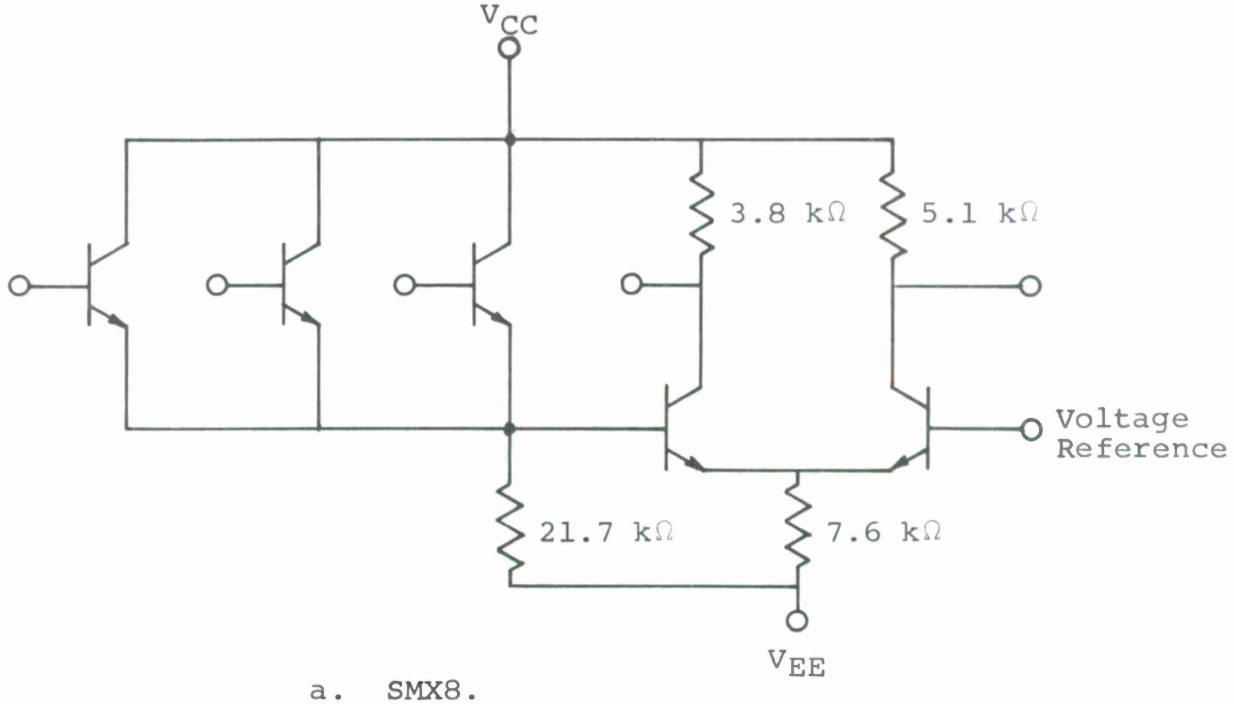
The Eleventh Interim Report stated that two new ECL gates were designed, both of which were to have relatively-low propagation delay-power products. The first microcircuit, designated SMX8, employs 0.1-mil geometry devices and tantalum resistors, and emphasizes low power dissipation. It was intended to operate at 1 mW dissipation at anticipated propagation delays of 1 to 2 ns. The microcircuit transistor has a single stripe emitter of 0.1 x 0.3 mil and a base area of 0.25 mil^2. A schematic diagram for the SMX8 is shown in Figure 31a.

The second microcircuit, designated SMX9, employs micron geometries and diffused resistors, and was designed to operate at very high speed (propagation delay expected to be less than 0.2 ns) with power dissipation of 35 to 40 mW. Signal swings are 800 mV. A schematic diagram for the SMX9 is shown in Figure 31b.

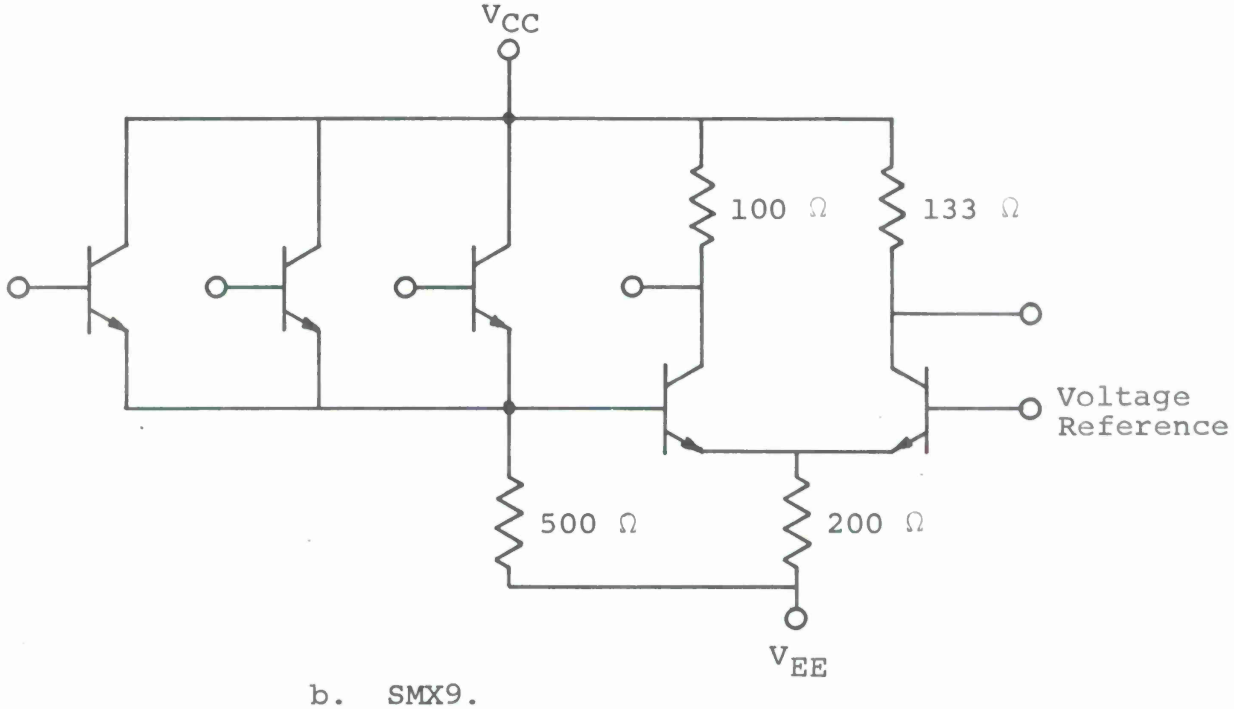
Both the SMX8 and SMX9 are 3-input gates, with emitter follower inputs and complementary outputs. Both employ two levels of metalization to minimize pad capacitances and to effect low capacitance crossovers.

7.1 SMX8 ECL GATE

Figure 32 is a photomicrograph of an SMX8. The first SMX8 microcircuits fabricated have been fully evaluated. Test results



a. SMX8.



b. SMX9.

Figure 31. Schematic diagrams for two new ECL gates.

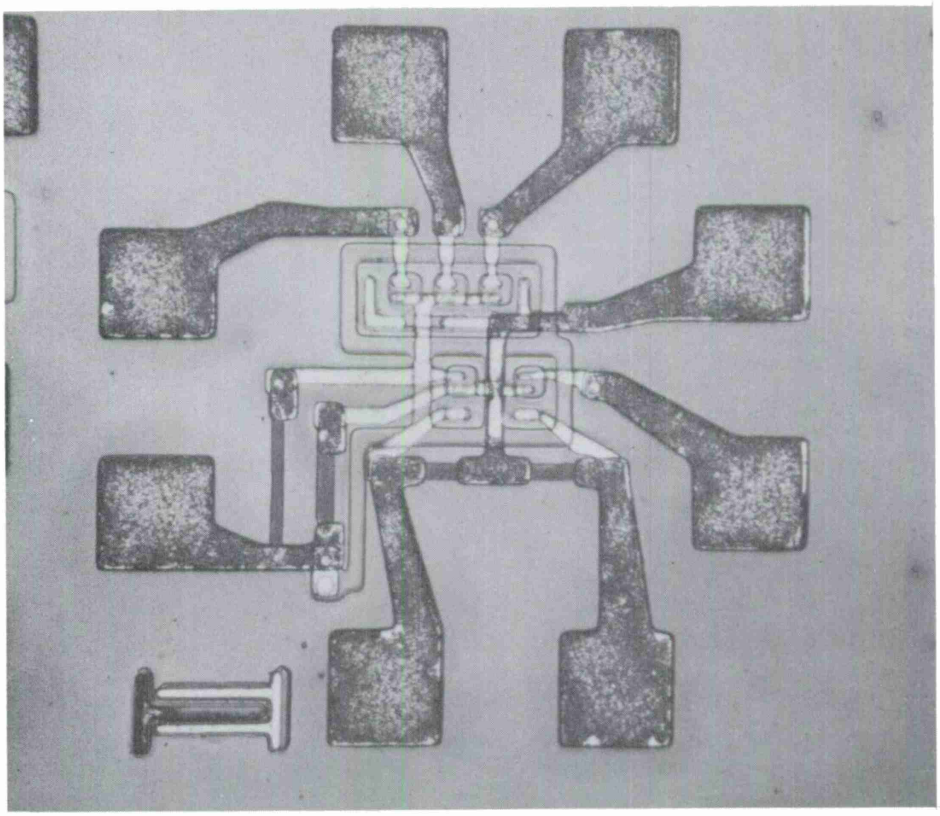


Figure 32. Photomicrograph of 1-mW, high-speed ECL gate (SMX8).

indicate that the performance goals of 1 mW power dissipation and 1 to 2 ns propagation delay were not fully achievable with this design. The lowest propagation delay that was obtained for 1 mW operation was 6.3 ns.

The speed-power curve shown in Figure 33 was obtained using microcircuits from a single wafer by stabilizing the microcircuit tantalum resistors in different parts of the wafer to different values. The fact that τ_{pd} falls as a function of increasing power indicates that the SMX8 microcircuits are load- or capacitance-limited in the region of 1-mW power dissipation. If the microcircuit were device-limited, τ_{pd} would increase with increased power dissipation. The speed limitation due to loading is not surprising since the load resistors are in the range of 4 to 5 kΩ. However, load capacitances were expected to be lower than indicated by the test data, especially since special measures were taken to minimize the capacitances. The special measures include the use of a very small transistor (0.03 $mils^2$ emitter, 0.25 $mils^2$ base area), Ta resistors having high sheet resistivity, and bilevel metalization wherein the resistors and pads are fabricated on the second level. Accurate determination of the raw chip delay was difficult due to the great sensitivity of the microcircuit to parasitic capacitances, including the capacitance of the measuring probes. However, ring oscillator measurements of

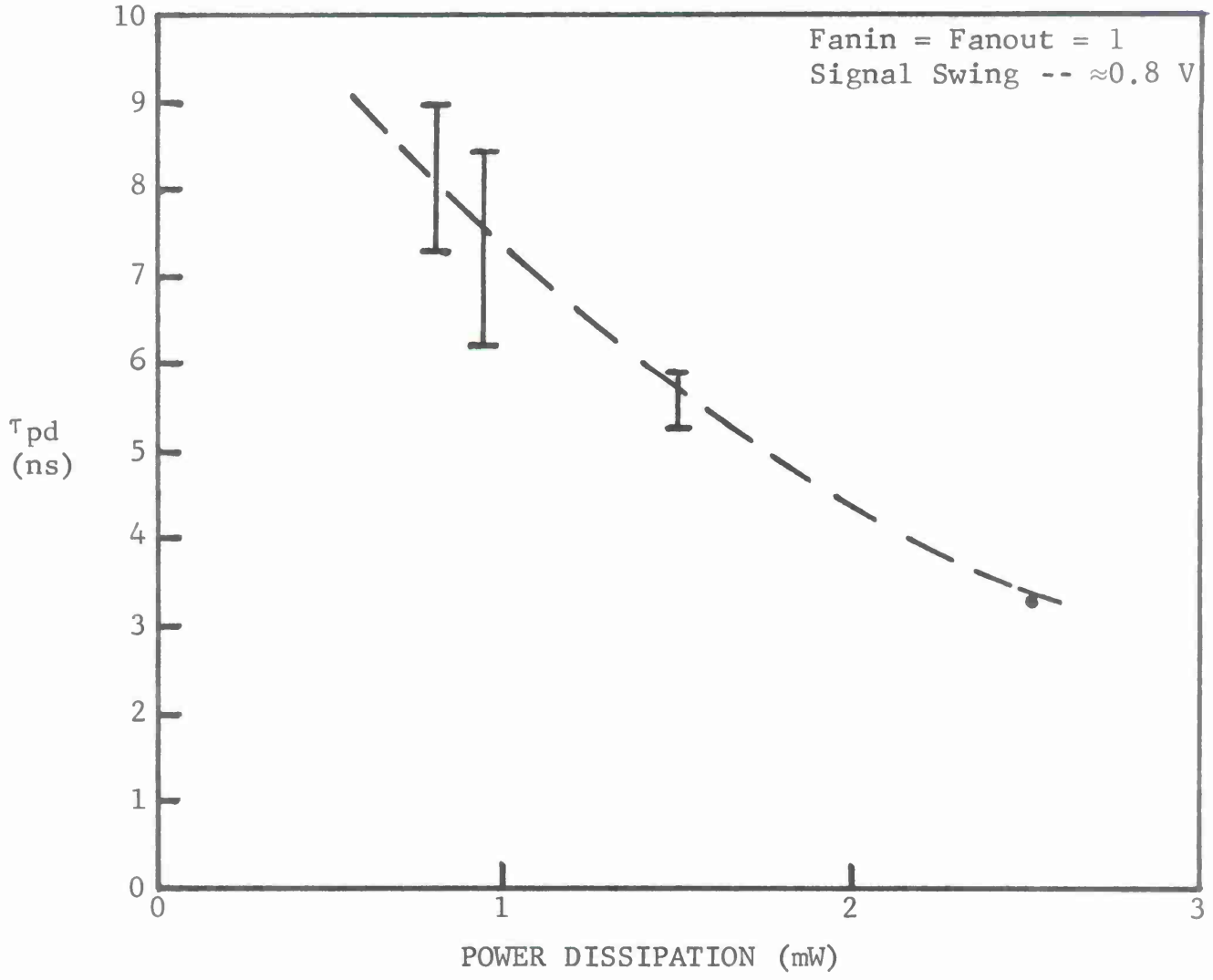


Figure 33. Propagation delay time versus power dissipation for the emitter follower input, complementary output, ultrasmall geometry ECL gate (SMX8).

propagation delays agreed with those obtained on individually packaged microcircuits.

7.2 SMX9 ECL GATE

Completion of SMX9 gate microcircuits has been delayed due to priority requirements of other phases of the program.

7.3 SMX12 ECL GATE

During this program, a 0.1-mil geometry high speed ECL microcircuit gate (designated SMX12) was designed as part of an experiment to evaluate computer-aided drafting as a method for reducing the layout design time for high speed microcircuits and microcircuit arrays. The SMX12 contains seven transistors, two diodes and seven resistors. Figure 34 is a photomicrograph of an SMX12; Figure 35 shows the schematic diagram of the SMX12.

From the circuit design aspect, the SMX12 differs from previously studied ECL gates in that it contains a built-in reference voltage network. Evaluations of this reference network will help in the design of future ECL arrays wherein inclusion of reference voltage networks will be valuable in reducing interconnection complexities by reducing the number of buss lines from three to two. Also, only a single power supply is required.

Die sort data obtained on fabricated wafers indicated circuit yields as high as 44%.

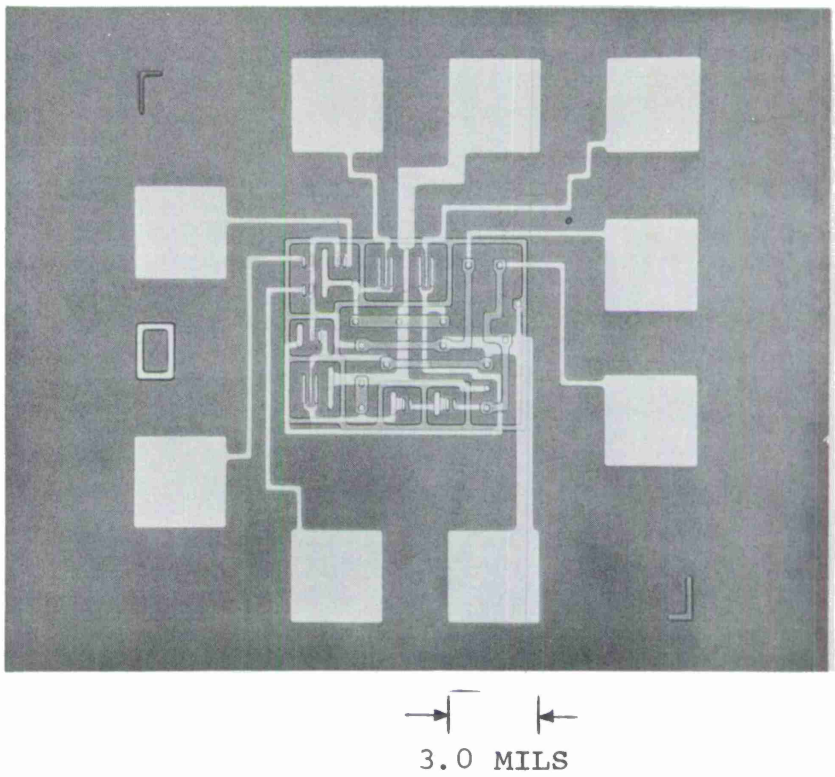


Figure 34. Photomicrograph of SMX12 high-speed 0.1-mil geometry ECL gate.

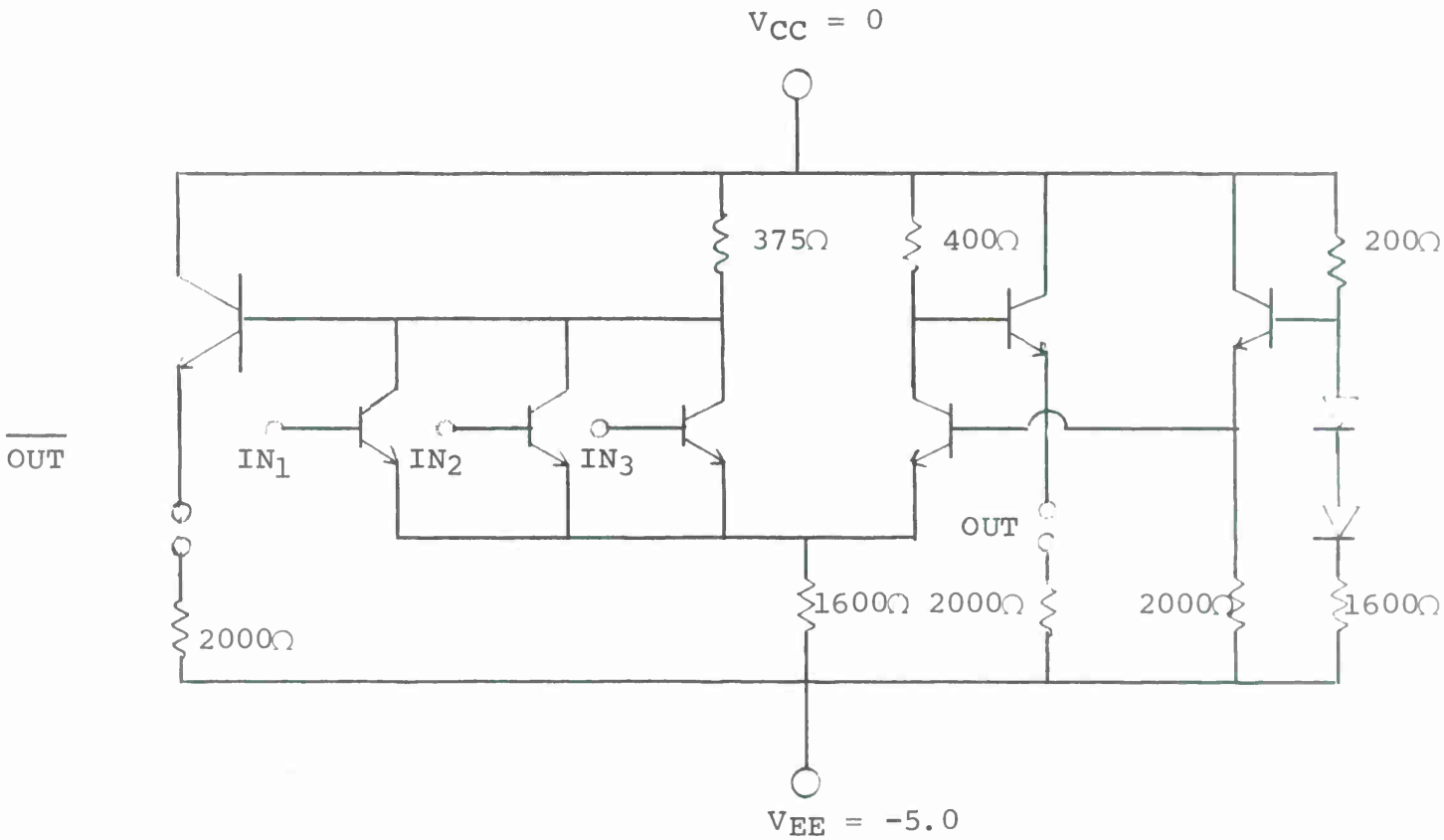
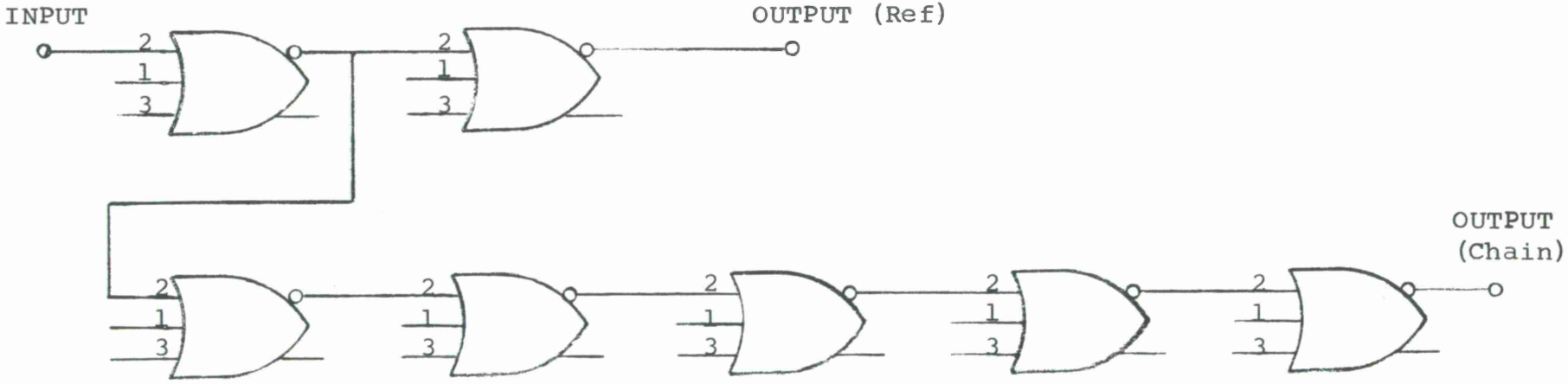


Figure 35. Schematic of SMX12 microcircuit.

The average propagation delay measured for the SMX12 microcircuit was 0.65 to 0.70 ns, while operating at an average power dissipation of 45 to 48 mW. Signal swing was 800mV. Figure 36 illustrates the method employed for measuring speed of the SMX12. Seven-gate chips were interconnected in a single package to form the gate-chain configuration shown in Figure 36. By subtracting the signal propagation delay measured through the reference path from the signal propagation delay measured through the test chain, the true propagation delay through four gate stages, unaffected by package environment and test apparatus, is measured. Note that in this test the emitter followers of the noninverted outputs are not powered. Figure 37 illustrates the waveforms of two separate gate chains, that were wired and tested in this manner.

The above evidence indicates that high-speed, high-yield microcircuit layout designs can be generated using computer-aided drafting techniques. Higher yields can be expected on future designs when certain refinements in the computer program and design rules are made. As an example, a major yield loss factor has been aluminum-to-aluminum shorts caused by non-optimum design of the metalization masks, partly due to design compromises necessitated by the present computer program.

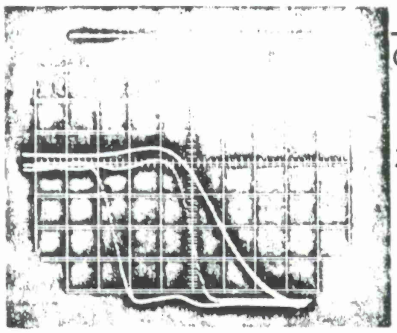


The average τ_{pd} of a single gate = $\frac{\tau_{pd}(\text{Chain}) - \tau_{pd}(\text{Ref})}{4}$.

Figure 36. Schematic diagram illustrating the technique employed to measure propagation delay time on SMX12 ECL gates.

CHAIN #1

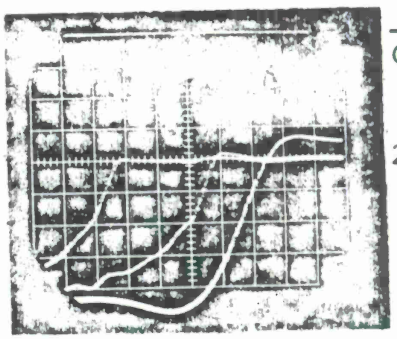
tpd+



1 ns/cm ←

OUT_{Chain} OUT_{Ref} IN

tpd-

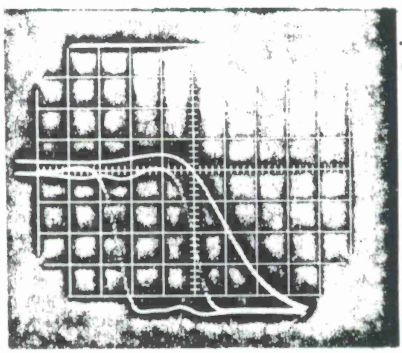


1 ns/cm ←

OUT_{Chain} OUT_{Ref} IN

CHAIN #2

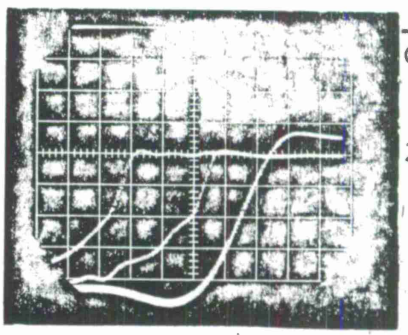
tpd+



1 ns/cm ←

OUT_{Chain} OUT_{Ref} IN

tpd-



1 ns/cm ←

OUT_{Chain} OUT_{Ref} IN

Figure 37. Output waveforms for SMX12 gate chains.

VIII - COMPUTER AIDED DRAFTING (CAD)

In the conventional mask making processes, much of the time necessary to produce the photomasks for a specific microcircuit or microcircuit array is the time used in layout design and in generation of artwork. It was believed that with computer aid, the time required for these operations could be reduced substantially. This reduction in mask generation time would significantly reduce turn-around time and very probably lower the cost. It was also believed that computer aid would result in a lower incidence of artwork errors, especially on complex masks containing repetitive patterns.

In a cooperative effort between Lincoln Laboratory and Philco-Ford, photomask layouts for a single ECL gate (Figure 34) and a complex ROM array (Figure 12) were designed using CAD techniques. This design effort was followed by generation of working masks and fabrication of the design structures. The purpose of this effort was to determine how the use of CAD techniques in the design of small-geometry, high-frequency microcircuits and arrays can affect turn-around time, cost and yield. The following sequence of steps was used to produce the indicated mask sets:

1. A designer generated the equivalent of a composite layout drawing and separate photomask drawings. This step

involved use of a Sylvania grid tablet and stylus, a computer (TX-2) which was programmed with appropriate design rules, and a CRT display. The coordinate data for patterns of these layouts were stored by the computer, and then later punched out on tape upon prescribed command.

2. The tape was fed into a commercial pattern generator which generated 10X reticles for each photomask drawing.
3. Each reticle was then processed into working photomasks using conventional microstepping techniques.

From the results of the CAD effort described above, we concluded that small-geometry (0.1 mil) microcircuits and arrays can be designed using CAD techniques and commercial pattern generation equipment. A substantial improvement in turn-around time is realized. For example, the total time required to produce completed photomasks for the SMX12 ECL gate was reduced by a factor of three to five compared to the conventional methods of photomask design and processing. Concerning layout design accuracies, no errors were found in either the simple SMX12 mask set or in the complex ROM mask set. Concerning yield, even though program limitations restricted optimum design in some parts of the SMX12, microcircuit yields at die sort ran as high as 44% on the first wafer lot that was processed. In addition, die sort yields of

functional ROM arrays ran as high as 37%. Concerning cost, there is difficulty at this time in assessing the level of improvement that might be realized if all operations were carried out on a commercial basis. However, within the limits of this specific CAD evaluation, which used a computer and a developed graphics capability of Lincoln Laboratory, there definitely was a reduction in overall cost to produce the SMX12 and the ROM.

IX - DELIVERIES

During the course of this program the following deliveries were made to Lincoln Laboratory:

1. Packaged samples of SMX8 Gates
2. Test transistors from the SMX8 Gates
3. Packaged samples of 3-Bit Parity Arrays
4. Two wafers containing functional 3-Bit Parity Arrays
5. Packaged samples of Read Only Memory Arrays
6. Packaged samples of SMX12 Gates
7. Packaged 9-Bit Parity Checker Subsystem assembled by face-down bonding techniques.

X - CONCLUSIONS

The generation of complex, high-speed digital microcircuit arrays ($\tau_{pd} \leq 1$ nsec/stage) requires a unique combination of monolithic microcircuit and multilevel interconnection techniques. Precise control of silicon material properties, diffusion processes, photolithography, photomask generation, and metalization processes is required to achieve the high yields (90 - 100%, depending upon microcircuit complexity) of shallow-diffused (0.5 μ) small-geometry (0.1 mil) transistors required to fabricate complex high-speed arrays at practical yields. An effective multilevel interconnection process is required to achieve high component densities ($\approx$10 mils^2/comp).

During this program, an array technology was developed which demonstrated transistor yields as high as 98 - 99%. Functional two-level arrays with as many as 256 transistors were fabricated. Extrapolations predict that the technology developed is capable of producing arrays with gate densities of 50 to 80.

A single-package high-speed digital subsystem, assembled by face-down bonding four complex arrays onto an interconnection substrate demonstrated the effectiveness of face-down bonding as a multichip assembly technique for high-speed systems. A speed improvement of 11% was obtained with a face-down bonded subsystem,

compared with an equivalent subsystem assembled by hand wiring discretely packaged chips.

In the interest of reducing power dissipation in high-speed ECL gates, a study was made of power dissipation properties of an ECL gate designed to operate at dissipation levels of 1 to 2 mW. It was found on fabricated gate structures that at these dissipation levels, propagation delay cannot be expected to be less than 3 to 6 nsec.

Work in conjunction with Lincoln Laboratory has demonstrated that computer aided drafting (CAD) techniques can be used to design accurate, complex, high-speed microcircuit array photomasks three to five times faster than with more conventional mask-making techniques. A high-speed ECL gate (τ_{pd} = 0.7 nsec) and a Read Only Memory (256 transistors) were fabricated to demonstrate the effectiveness of the method.

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13. ABSTRACT

A research and development program was directed toward the development of fabrication technologies for high-speed computer subsystems. High-yield technologies for fabricating high-speed, high-density microcircuit and two-level microcircuit array structures have been developed and demonstrated. Design requirements for small-geometry three-level arrays have also been established. Multichip high-speed LSI subsystems have been assembled by face-down bonding, and characterized for speed and thermal properties. Computer aid has been incorporated into a system for designing and generating photomasks for complex high-speed microcircuits. A simple high-speed ECL gate and a complex, high-speed, high-density transistor Read-Only Memory were successfully designed and fabricated to demonstrate the technique.

14. KEY WORDS

Microcircuit arrays
Large-scale integration (LSI)
Read-Only Memory (ROM)
Multilevel interconnection
Computer-aided drafting (CAD)
Face-down bonding